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Faculty of Engineering
Computer Engineering Department

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in Computer Engineering

**Design and Implementation of High-Speed Custom
Instruction Architecture for Fast Fourier Transform on
FPGA-based NIOS II Embedded Processor**

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Abstract

This project presents the design and implementation of a custom instruction for the butterfly operation within the Decimation-In-Time (DIT) Fast Fourier Transform (FFT) algorithm, utilizing the NIOS II processor in an FPGA-based environment. The motivation behind this work stems from the computational intensity of FFT algorithms, which are pivotal in various digital signal processing (DSP) applications. Traditional software implementations on general-purpose processors often fall short in terms of speed. By leveraging the reconfigurability of FPGAs and the flexibility of NIOS II soft core processors, the proposed solution offering a hybrid approach that combines software and hardware optimization. This method involves designing a custom instruction specifically for the butterfly operation, a critical component of the FFT algorithm, to accelerate the computation. Compare the performance of a non-custom implementation with the hybrid approach that utilizes the custom instruction. Experimental results demonstrate a significant reduction in execution time when the custom instruction is employed. The conclusions drawn from this research work highlights the benefits of integrating hardware accelerators in FPGA-based systems to achieve substantial performance improvements in signal processing applications. This work showcases the potential of hardware-software co-design in optimizing computationally intensive algorithms, ultimately contributing to more efficient and faster processing solutions. Performance evaluations are conducted to compare the execution time of the custom instruction implementation against a conventional non-custom approach. The results indicate a significant improvement in execution speed, since with the custom instruction achieving a reduction in execution time by approximately 57%, the custom instruction has 0.142s comparing with 0.333s in non-custom instruction.

Keywords: Custom instruction, Fast Fourier Transform, NIOS II processor, FPGA, digital signal processing, hardware acceleration, butterfly operation, performance optimization.

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Lastly, I am truly grateful to all my family and friends for their unwavering support, belief in my abilities, and willingness to lend a helping hand, your support and camaraderie have made this journey more enjoyable.

Dedication

This work is dedicated to my beloved family, whose unwavering support and love have been the foundation of my academic journey.

To my parents, Ali Albakosh and Samira Aljourni, I am profoundly grateful for your sacrifices and encouragement. Your belief in my potential has provided me with the strength to pursue my education and research with passion and determination. You have instilled in me the values of hard work, perseverance, and integrity, which have guided me through the challenges I faced during my studies. Your constant support during moments of doubt and your ability to celebrate my achievements, no matter how small, have motivated me to strive for excellence.

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1.Introduction

The Fast Fourier Transform (FFT) is a fundamental algorithm in digital signal processing (DSP) that plays a crucial role in analyzing the frequency components of signals. Its applications span a wide range of fields, including telecommunications, audio processing, image analysis, and biomedical engineering. By transforming a sequence of complex numbers from the time domain to the frequency domain, the FFT enables efficient signal analysis and manipulation, which is essential for modern technological advancements. However, the computational complexity associated with FFT, particularly when dealing with large datasets, presents significant challenges that can hinder real-time processing capabilities.

The primary problem related to FFT computations lies in their inherent computational intensity. As the size of the input data increases, the time required for computation can grow exponentially, leading to performance bottlenecks that can severely impact the effectiveness of real-time applications. For instance, in telecommunications, delays in signal processing can degrade performance and user experience, while in medical imaging, slow processing times can hinder timely diagnosis and treatment. These inefficiencies underscore the critical need for optimized solutions that can enhance the performance of FFT computations, particularly in scenarios where rapid analysis and response are paramount.

Addressing these challenges is of utmost importance, as optimizing FFT computations not only improves the performance of existing systems but also opens the door to new applications and innovations in digital signal processing. Recent advancements in hardware architectures, particularly the use of custom instructions in programmable processors like the Nios II, present promising avenues for tackling these issues. By leveraging the capabilities of custom instructions, developers can accelerate FFT computations, significantly improving performance and resource utilization. This project aims to explore and implement various strategies to optimize FFT computations, ultimately enhancing the efficiency and effectiveness of digital signal processing in real-time applications.

1.2. Literature Review

Recent literature has proposed several solutions to enhance the performance of the Fast Fourier Transform (FFT) algorithm, focusing on various techniques that leverage both hardware and software optimizations. One prominent approach is hardware acceleration with FPGAs. Field-Programmable Gate Arrays (FPGAs) have gained popularity for implementing FFT algorithms due to their inherent parallel processing capabilities. Research has demonstrated that FPGAs can achieve significant speedups compared to traditional software implementations running on

general-purpose processors. For instance, studies indicate that the parallel architecture of FPGAs allows for simultaneous execution of multiple butterfly operations, leading to substantial reductions in computation time. Customizing the hardware for specific applications enables optimizations such as pipelining and resource sharing, which further enhance performance. Additionally, FPGA implementations can be tailored to specific FFT sizes, optimizing resource usage and minimizing latency, making them particularly suitable for real-time applications like telecommunications and audio processing. Notable examples include Kumar's work, which showcased a 4x speedup in FFT computation on an FPGA compared to a software implementation on a CPU [1].

Another effective method for optimizing FFT computations is custom instruction design. The integration of custom instructions into processors like the NIOS II allows developers to create specific operations tailored for the FFT algorithm, particularly for the butterfly computations central to the Decimation-In-Time FFT. By designing custom instructions that execute these butterfly operations directly in hardware, developers can significantly reduce the number of clock cycles required for FFT calculations, which is critical for applications requiring real-time processing. Research by Zhang demonstrated a 30% reduction in execution time for FFT computations on the NIOS II processor through the use of custom instructions [2]. Moreover, custom instructions can lead to a decrease in code size, as frequently used operations can be encapsulated within a single instruction, which is particularly beneficial in embedded systems with limited memory resources.

Optimized memory access patterns have also been shown to significantly improve the performance of FFT implementations. Studies indicate that inefficient memory access can lead to increased latency and reduced throughput, especially in large FFT computations. Techniques such as pipelining, cache optimization, and data locality management have been proposed to enhance memory access efficiency. For example, pipelining allows for overlapping computation and data transfer, minimizing idle time and maximizing resource utilization. Liu's research demonstrated that optimizing memory access patterns resulted in a 25% performance improvement in FFT implementations [3]. Efficient data flow management, such as using block-based processing or tiling techniques, can help reduce cache misses and improve overall memory bandwidth utilization, which is crucial for handling large datasets efficiently.

Lastly, hybrid approaches that combine software and hardware techniques have gained traction as a means to optimize FFT computations. These approaches leverage the flexibility of software while utilizing the speed of hardware acceleration, resulting in balanced performance improvements. Some researchers propose using software to handle control logic and data management while offloading computationally intensive tasks, such as butterfly operations, to

custom hardware or FPGAs. This separation of concerns allows for more efficient resource use and can lead to significant performance gains. Studies, such as those conducted by Wang, have demonstrated that hybrid implementations can achieve up to a 40% improvement in execution time compared to pure software implementations [4]. By combining the strengths of both software and hardware, hybrid approaches can adapt to varying application requirements and provide a more versatile solution for FFT computations.

While these solutions show promise, they often focus on specific aspects of FFT optimization without comprehensively integrating the benefits of custom instruction design.

1.3. Contribution of Proposed Solution

The contributions of this proposed solution are as follows:

1. **Performance Enhancement:** By offloading the butterfly operation to a custom instruction executed in hardware, we can significantly reduce execution time compared to traditional software implementations.
2. **Resource Optimization:** The custom instruction is designed to utilize FPGA resources efficiently, allowing for more complex operations to be performed within the same hardware constraints.
3. **Flexibility and Scalability:** The NIOS II processor's configurability allows for easy adaptation of the custom instruction to various DSP applications, making it a versatile solution for future developments.
4. **Real-Time Processing Capability:** The hardware acceleration provided by the custom instruction enables real-time processing of signals, which is essential for applications in various fields, including telecommunications, audio and video processing, medical imaging, and control systems.

1.4. Overview of Subsequent Chapters

The subsequent chapters of this report will be organized as follows:

Chapter 2: Experiment Environments: This chapter represents the all hardware and development environments that used in the project.

Chapter 3: Methodology: This chapter represents detail the methodologies employed in the project, including the design of custom instructions, system architecture definition,

and software development processes. It will outline the tools and techniques used to achieve the project objectives.

Chapter 4: Results and Discussions: This chapter presents the implementation of the FFT algorithm on the NIOS II processor, including the integration of custom instructions. It showcases the results of the performance evaluation, highlighting the improvements achieved.

Chapter 5: Conclusion and Future Work: The final chapter will summarize the key findings of the research, reiterating the importance of optimizing FFT computations. It will also propose directions for future work, suggesting areas where further enhancements and research could be pursued.

2. Experiment Environment

2.1. Hardware Environment

In this project, various hardware environments are utilized to optimize the implementation and performance of the Fast Fourier Transform (FFT) algorithm. The following sections detail the key hardware components and environments that contribute to the overall functionality and efficiency of the project.

2.1.1. DE2i-150 board

The DE2i-150 board is an advanced educational and development platform designed by Intel (formerly Altera) for prototyping and experimentation with digital designs. It features a range of components and interfaces that make it suitable for various applications, including digital signal processing, embedded systems, and hardware design education. The DE2i-150 board as shown in Figure 2-1 is particularly notable for its integration of a Field-Programmable Gate Arrays (FPGA), peripherals, and user interface components, providing a comprehensive environment for developing and testing custom applications [5].

The Architecture of the DE2i-150 Board:

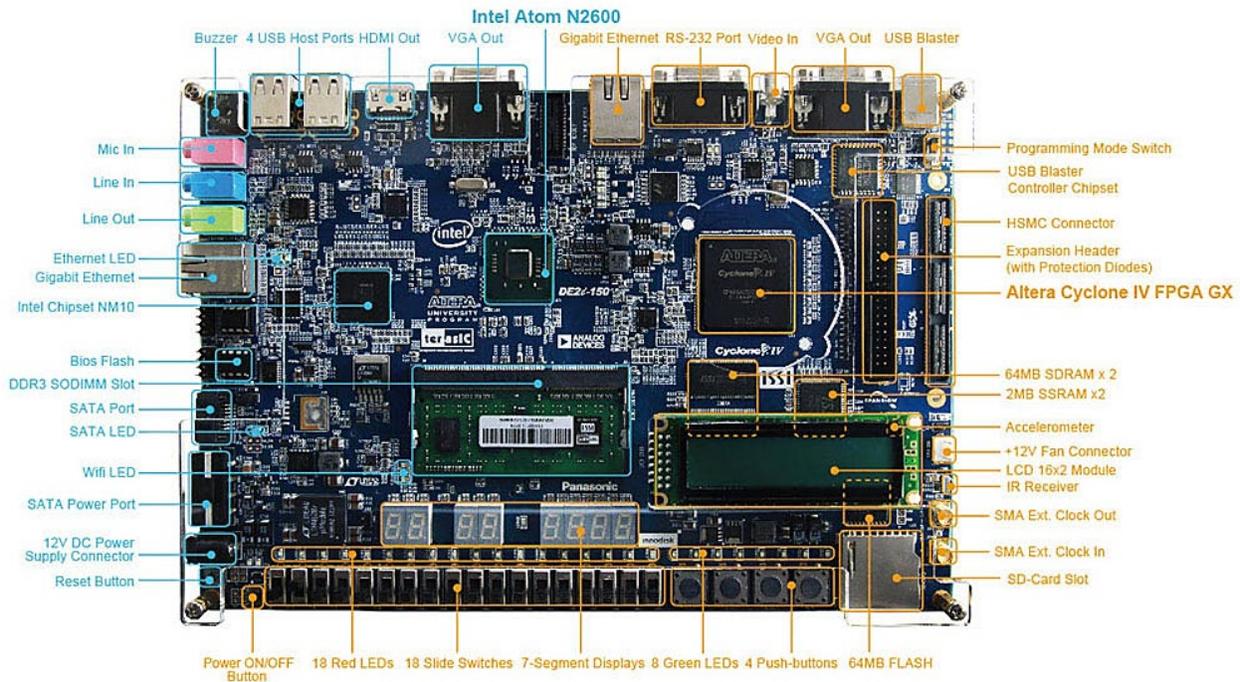


Figure 2-1 The DE2i-150 board

1. **FPGA Component:** At the heart of the DE2i-150 board is the **Altera Cyclone IV FPGA**. This FPGA is a low-cost, low-power device that offers a balance of performance and resource availability. The Cyclone IV FPGA provides a significant number of logic elements, memory blocks, and digital signal processing (DSP) capabilities, making it suitable for a wide range of applications.
2. **Memory:** The board includes various types of memory, such as SDRAM and Flash memory. The **SDRAM** is used for temporary data storage during processing, while the **Flash memory** provides non-volatile storage for configuration and user data.
3. **I/O Interfaces:** The DE2i-150 board is equipped with multiple input/output interfaces, including:
 - **USB:** For communication with external devices and programming the FPGA.
 - **HDMI:** For video output, allowing for the display of graphical content.
 - **VGA:** For connecting to monitors and displaying output.
 - **Audio Interfaces:** For input and output of audio signals, facilitating multimedia applications.
 - **GPIO:** General-purpose input/output pins for interfacing with various sensors and actuators.
4. **User Interface Components:** The board features several user interface components, including:
 - **LEDs:** For visual feedback and status indicators.
 - **Switches:** For user input and configuration.
 - **Seven-Segment Displays:** For displaying numerical values and status information.
5. **Expansion Connectors:** The DE2i-150 board includes expansion connectors that allow for the integration of additional peripherals and modules. This feature enhances the board's versatility and enables users to customize their setups for specific applications.

2.1.2. Field-Programmable Gate Arrays

Field-Programmable Gate Arrays are integrated circuits that can be configured by the user after manufacturing, allowing for a high degree of flexibility in hardware design. FPGAs are widely used

in various applications, including digital signal processing, telecommunications, automotive systems, and embedded systems. Their programmability enables designers to implement custom digital circuits tailored to specific tasks, making them a powerful tool in modern electronics [6].

An FPGA has a regular structure of logic cells or modules and interlinks which is under the developers and designers complete control. The FPGA is built with mainly three major blocks such as Configurable Logic Block (CLB), I/O Blocks or Pads and Switch Matrix/ Interconnection Wires as shown in Figure 2-2. Each block will be discussed below in brief.

- **CLB:** These are the basic cells of FPGA. It consists of one 8-bit function generator, two 16-bit function generators, two registers (flip-flops or latches), and reprogrammable routing controls (multiplexers). The CLBs are applied to implement other designed function and macros. Each CLBs have inputs on each side which makes them flexible for the mapping and partitioning of logic.
- **I/O Pads or Blocks:** The Input/Output pads are used for the outside peripherals to access the functions of FPGA and using the I/O pads it can also communicate with FPGA for different applications using different peripherals.
- **Switch Matrix/ Interconnection Wires:** Switch Matrix is used in FPGA to connect the long and short interconnection wires together in flexible combination. It also contains the transistors to turn on/off connections between different lines.

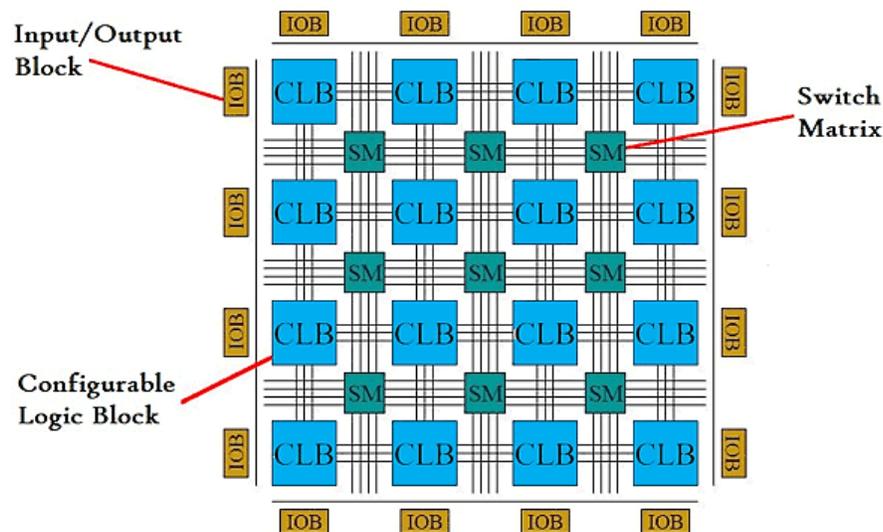


Figure 2-2FPGA block diagram

FPGAs can be reprogrammed to implement different functions or algorithms, making them suitable for a wide range of applications. This flexibility allows for rapid prototyping and iterative design processes.

The architecture of FPGAs enables parallel processing of multiple tasks, which can significantly enhance performance for applications that require high-speed data processing, such as digital signal processing and real-time analysis.

Designers can create custom hardware solutions tailored to specific requirements, optimizing performance and resource utilization. This customization is particularly advantageous in applications where off-the-shelf solutions may not meet performance criteria.

FPGAs can reduce development costs by allowing for hardware changes through software updates rather than requiring new hardware designs. This is especially beneficial for low to medium volume production runs.

The ability to quickly reconfigure FPGAs allows for faster development cycles. Designers can test and iterate on their designs without the delays associated with traditional hardware development.

In projects involving digital signal processing, such as FFT implementations, FPGAs provide the necessary performance to handle real-time data processing. Their parallel processing capabilities allow for efficient handling of complex algorithms. The ability to implement custom logic tailored to the specific requirements of the project makes FPGAs ideal for optimizing performance. For instance, custom instructions can be added to accelerate FFT computations, enhancing overall efficiency. FPGAs can host soft processors like the Nios II, allowing for a combination of hardware and software processing. This integration enables the execution of complex algorithms while leveraging the flexibility of FPGA architecture. FPGAs can easily scale to accommodate different input sizes and complexities, making them suitable for applications where the size of the data may vary. This scalability is crucial in projects that require adaptability to changing requirements. Using FPGAs for prototyping allows developers to test their designs in real-world scenarios without the need for extensive hardware changes. This cost-effectiveness is particularly beneficial in research and development projects.

2.1.3. NIOS II Processor

The Nios II processor is a 32-bit RISC (Reduced Instruction Set Computing) soft processor core developed by Intel (formerly Altera) for implementation in Field-Programmable Gate Arrays (FPGAs). It is designed to be highly configurable, allowing developers to tailor the processor architecture to meet specific application requirements. The Nios II processor is particularly well-suited for embedded systems and digital signal processing applications due to its flexibility, performance, and resource efficiency [7]. Nios II Processor Core Block Diagram shows in Figure 2-3.

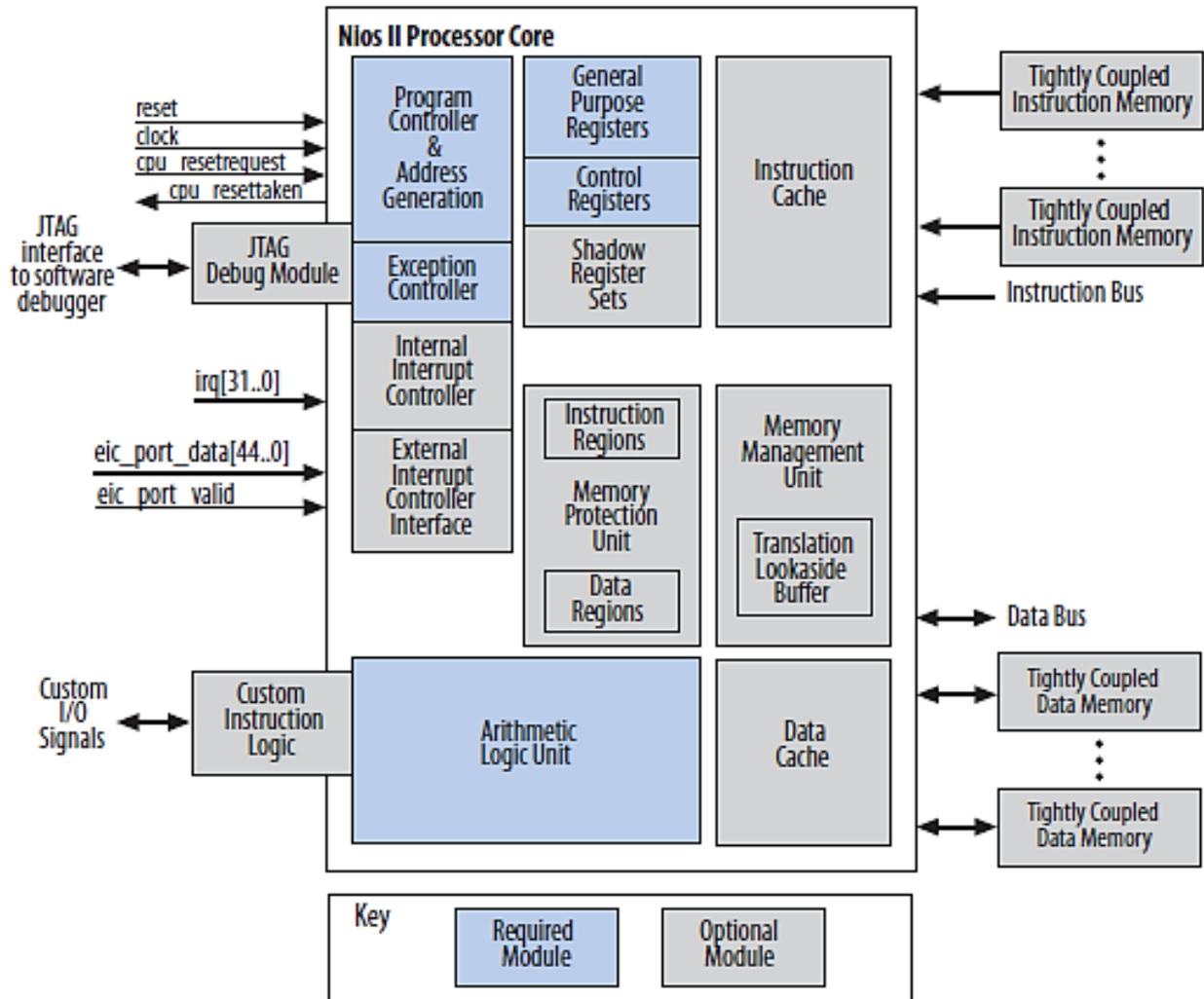


Figure 2-3 Nios II Processor Core Block Diagram

The architecture of the Nios II processor is modular and customizable, which allows designers to optimize it for various tasks. Key components of the Nios II architecture include:

1. Core Components:

- **Arithmetic Logic Unit (ALU):** Executes arithmetic and logical operations.
- **Registers:** A set of general-purpose registers that facilitate data storage and manipulation.
- **Instruction Fetch Unit:** Responsible for fetching instructions from memory.

2. **Configurability:**

- The Nios II processor can be configured with different data widths (16-bit or 32-bit), memory interfaces, and peripheral interfaces, enabling designers to create a processor that fits their specific needs.
- Custom instructions can be added to enhance performance for specific algorithms, such as the Fast Fourier Transform (FFT).

3. **Memory Architecture:**

- The processor supports various memory types, including SRAM, SDRAM, and ROM, allowing for flexible memory configurations.
- It can be connected to local memory or external memory interfaces, depending on the application requirements.

4. **Pipeline Architecture:**

- The Nios II processor utilizes a pipelined architecture, which allows for overlapping instruction execution. This improves throughput and overall performance by enabling multiple instructions to be processed simultaneously.

5. **Bus Interfaces:**

- The processor can communicate with various peripherals and components through standard bus interfaces, such as Avalon and Wishbone, facilitating easy integration into larger systems.

The Nios II Processor have the ability to configure the processor architecture allows developers to optimize it for specific applications, ensuring that the processor meets performance and resource requirements. As a soft processor, the Nios II can be implemented on FPGAs, allowing for efficient use of logic elements and memory resources. This is particularly advantageous in embedded systems where resource constraints are common. The Nios II processor can achieve high performance through its pipelined architecture and the ability to add custom instructions. This is especially beneficial for computationally intensive tasks such as digital signal processing. The Nios II processor can be easily adapted to a wide range of applications, from simple control tasks to complex signal processing algorithms. This flexibility makes it a popular choice in various industries, including telecommunications, automotive, and consumer electronics. Intel provides a comprehensive suite of development tools, including Quartus Prime and the Nios II Software Build Tools, which facilitate the design, simulation, and implementation of Nios II-based systems.

The reasons for Using Nios II in FFT Implementations:

- **Optimized Performance:** The Nios II processor's ability to incorporate custom instructions allows for significant performance improvements in FFT computations. Custom instructions can be designed to accelerate specific operations within the FFT algorithm, reducing execution time and enhancing overall efficiency.
- **Real-Time Processing:** The Nios II processor is well-suited for applications requiring real-time processing, such as signal analysis and manipulation. The reduced latency achieved through custom instructions is crucial for applications in telecommunications and audio processing, where timely responses are essential.
- **Integration with FPGA:** Implementing the FFT algorithm on the Nios II processor within an FPGA allows for parallel processing capabilities, which can further enhance performance. The flexibility of the FPGA enables designers to optimize the hardware for specific FFT sizes and configurations.
- **Scalability:** The Nios II processor can easily scale to accommodate different FFT lengths and complexities, making it adaptable to various signal processing tasks. This scalability is important in applications where the size of the input data may vary.
- **Cost-Effectiveness:** By using a soft processor like Nios II, developers can reduce costs associated with hardware development. The ability to configure and reconfigure the processor as needed allows for iterative design improvements without the need for additional hardware.

2.1.4. Custom Instructions

One of the standout features of Nios II is the ability to incorporate **custom instructions**, which allow developers to extend the standard instruction set architecture (ISA) to optimize performance for specific applications. Custom instructions enable the implementation of specialized operations directly in hardware, resulting in significant enhancements in execution speed and resource utilization [3].

The advantages of using custom instructions in the Nios II processor are manifold:

- **Performance Optimization:** Custom instructions can dramatically reduce execution time for critical operations, enabling applications to meet real-time processing requirements, particularly in digital signal processing (DSP) and embedded systems.

- **Resource Efficiency:** By offloading frequently used operations to custom instructions, developers can optimize the use of FPGA resources, allowing for more efficient designs that accommodate additional functionality without exceeding resource limits.
- **Flexibility:** The ability to define and modify custom instructions allows developers to adapt their designs to changing application requirements without needing to redesign the entire processor.
- **Reduced Code Size:** Custom instructions can encapsulate complex operations, leading to smaller code sizes and improved overall system performance.

The Figure 2-4 shows Hardware Block Diagram of a Nios II Custom Instruction [8].

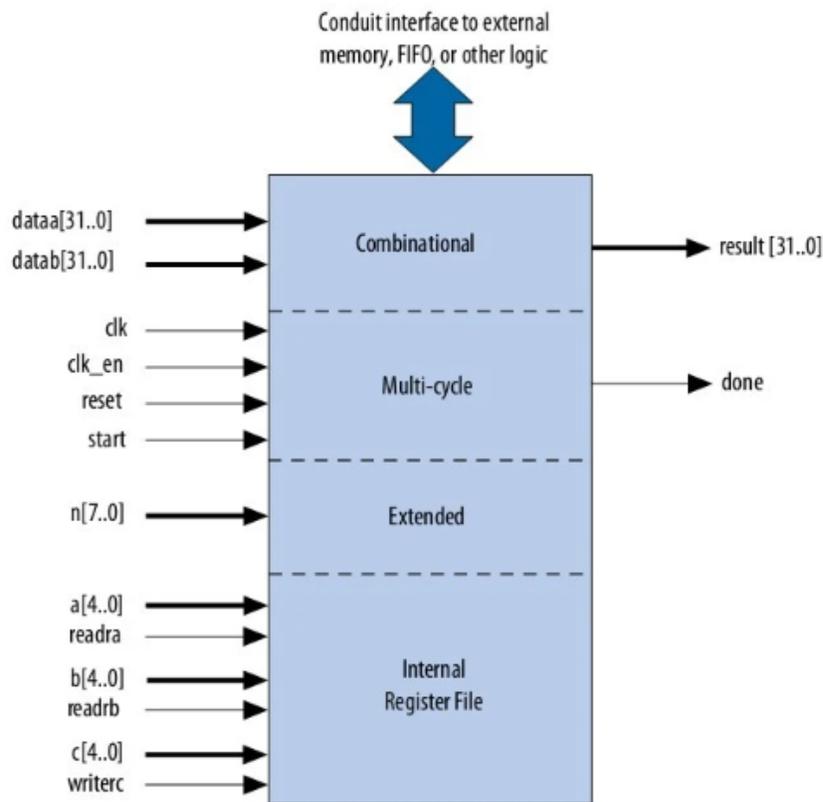


Figure 2-4 Hardware Block Diagram of a Nios II Custom Instruction

The custom logic blocks can be implemented using either one or a combination of the following four

Options.

1. Combinatorial Logic

Combinatorial logic custom instructions are designed to execute operations that depend solely on the current inputs without any memory elements as shown in Figure 2-5 . These

instructions allow for the implementation of complex logic functions directly in hardware, enabling rapid execution of tasks such as arithmetic operations, data selection, and signal manipulation. By utilizing combinatorial logic, developers can optimize performance for applications requiring immediate response to input changes, making it particularly useful in digital signal processing and control systems.



Figure 2-5 Combinatorial logic custom instructions block diagram

2. Multi-cycle Logic

Multi-cycle logic custom instructions are tailored to perform operations that require multiple clock cycles to complete. This approach allows for more complex computations to be broken down into simpler steps, which can be executed sequentially. By using multi-cycle logic, developers can optimize resource utilization, as the same hardware can be reused across different cycles for various operations. This is especially beneficial in scenarios where certain tasks are too complex to be executed in a single cycle, allowing for enhanced performance without the need for additional resources.

3. Parameterization

Parameterization in the context of custom instructions refers to the ability to define certain aspects of the instruction as adjustable parameters. This feature allows developers to create flexible and reusable instruction designs that can be tailored to specific application requirements. By parameterizing custom instructions, designers can easily adapt their implementations to varying data sizes, operation types, or performance criteria without extensive redesign. This flexibility enhances the efficiency of the development process and allows for rapid adaptation to changing project needs.

4. User-defined Ports

User-defined ports custom instructions provide a mechanism for designers to specify custom input and output interfaces for their instructions. This feature allows for tailored communication pathways between the processor and external components, enabling greater flexibility in how modules interact. By defining user-specific ports, developers can create modular and reusable instruction sets that meet the unique requirements of their applications. This capability is particularly valuable in complex designs, where standard

interfaces may not suffice, allowing for optimized integration with various hardware components.

In this project, **combinational custom instructions** are of particular importance due to their ability to execute specific operations rapidly and efficiently. By implementing combinational custom instructions, we can significantly accelerate the execution of critical algorithms, such as the Fast Fourier Transform (FFT). This optimization is essential for meeting the real-time processing demands of the application, allowing for faster signal analysis and manipulation.

The use of combinational custom instructions not only enhances performance but also improves resource utilization within the FPGA. By encapsulating complex operations into a single instruction, we can reduce the overall code size and streamline the processing workflow, ultimately leading to a more efficient and effective system design.

These instructions are designed to execute tasks based solely on the current inputs, without relying on any previous states or memory elements. This characteristic enables immediate response to input changes, making combinatorial logic particularly effective for applications that require high-speed processing and real-time performance.

The functionality of Combinatorial Logic Custom Instructions is:

- **Single-Cycle Execution:** Combinatorial logic custom instructions are executed in a single clock cycle, which means that the output is available immediately after the inputs are applied. This rapid execution is essential for applications that demand low latency.
- **Direct Hardware Implementation:** By implementing logic functions directly in hardware, combinatorial logic custom instructions can perform complex operations such as arithmetic calculations, data selection, and bit manipulation efficiently. This direct implementation reduces the overhead associated with executing multiple standard instructions.
- **Flexibility in Design:** Developers can define custom combinatorial logic instructions tailored to specific application requirements. This flexibility allows for the optimization of critical algorithms, enhancing overall system performance.

The advantages of using Combinatorial Logic Custom Instructions is:

- **Performance Improvement:** The primary advantage of combinatorial logic custom instructions is the significant reduction in execution time for critical operations. By executing tasks in a single cycle, these instructions can enhance the responsiveness of applications, particularly in real-time processing scenarios such as digital signal processing (DSP) and control systems.

- **Resource Efficiency:** Combinatorial logic custom instructions allow for efficient use of FPGA resources. By consolidating multiple operations into a single instruction, developers can minimize the number of logic elements required, leading to a more compact and efficient design.
- **Reduced Code Complexity:** By encapsulating complex logic operations within a single custom instruction, developers can simplify their code. This reduction in code complexity not only makes the design easier to understand and maintain but also minimizes the potential for errors during implementation.
- **Enhanced Throughput:** The ability to execute multiple operations simultaneously through combinatorial logic can lead to increased throughput in applications that require high data rates. This is particularly beneficial in scenarios such as video processing or high-speed data acquisition.
- **Lower Power Consumption:** By reducing the number of clock cycles needed to perform operations, combinatorial logic custom instructions can also lead to lower power consumption. This is especially important in embedded systems where power efficiency is a critical consideration.

In the context of this project, combinatorial logic custom instructions are utilized to optimize the performance of the Fast Fourier Transform (FFT) algorithm. The FFT is a computationally intensive operation commonly used in signal processing applications, and its efficiency is paramount for real-time analysis.

By implementing combinatorial logic custom instructions specifically designed for the FFT, we can achieve the following:

- **Accelerated Processing:** The custom instructions allow for rapid execution of FFT computations, significantly reducing the time required for signal analysis and manipulation.
- **Improved Resource Utilization:** The efficient design of combinatorial logic custom instructions ensures that FPGA resources are utilized optimally, allowing for additional functionalities to be integrated without exceeding resource limits.
- **Real-Time Performance:** The immediate response capabilities of combinatorial logic custom instructions are essential for meeting the real-time processing demands of the project, ensuring timely analysis and response to input signals.

Combinatorial logic custom instructions are a powerful tool for optimizing the performance of the Nios II processor in applications requiring high-speed processing and low latency. Their ability to execute operations in a single cycle, coupled with advantages such as resource efficiency and reduced code complexity, makes them particularly valuable in this project. By leveraging

combinatorial logic custom instructions, we can enhance the efficiency of the FFT algorithm, ultimately leading to improved performance in real-time signal processing applications

2.1.5. On-Chip Memory

On-chip memory, also known as embedded memory, refers to memory that is integrated directly within the silicon chip of the processor or FPGA. This type of memory is typically used for high-speed data storage and access, as it is located close to the processing units, minimizing latency [9]. On-chip memory can take various forms, including:

1. **Registers:** Small storage locations within the processor that hold data temporarily for immediate processing.
2. **Cache Memory:** A small amount of high-speed memory that stores frequently accessed data and instructions, allowing for faster retrieval compared to accessing main memory.
3. **Block RAM (BRAM):** Dedicated memory blocks available in FPGAs that can be configured for various data widths and depths, providing flexibility for different applications.

On-chip memory offers significantly faster access times compared to external memory solutions, making it ideal for applications requiring quick data retrieval and processing.

The proximity of on-chip memory to the processing units reduces the time it takes to access data, which is critical for real-time applications.

Accessing on-chip memory consumes less power than accessing off-chip memory, which is essential in battery-operated and energy-sensitive applications.

2.1.6. SDRAM Memory

SDRAM (Synchronous Dynamic Random Access Memory) is a type of external memory that synchronizes its operation with the system clock. SDRAM is widely used in computer systems and embedded applications due to its ability to provide high-speed data access and large storage capacity. SDRAM operates by storing data in capacitors, which need to be refreshed periodically to maintain the stored information [10].

SDRAM can provide larger storage capacities compared to on-chip memory, making it suitable for applications that require significant amounts of data storage. SDRAM is generally less expensive per bit compared to on-chip memory, making it a cost-effective solution for applications that require large memory sizes. SDRAM can be used for various applications, from general-purpose computing to specialized embedded systems, due to its adaptability and scalability.

In the context of this project, both on-chip memory and SDRAM memory are utilized to leverage their respective advantages:

1. **On-Chip Memory:**

- On-chip memory is used for storing critical data and instructions that require fast access, such as intermediate results of computations and frequently used variables. The low latency and high speed of on-chip memory are essential for ensuring that the processing tasks, such as those involved in the Fast Fourier Transform (FFT) algorithm, are executed efficiently and in real-time.

2. **SDRAM Memory:**

- SDRAM is employed for storing larger datasets and buffers that not fit into on-chip memory. For instance, in applications involving signal processing, SDRAM can hold extensive input data or processed results that need to be accessed less frequently but require substantial storage capacity. The ability to refresh and manage larger volumes of data makes SDRAM a suitable choice for handling the demands of complex algorithms and larger datasets.

In summary, the use of both on-chip memory and SDRAM memory in this project allows for an optimal balance between speed, capacity, and efficiency. On-chip memory provides the high-speed access necessary for real-time processing, while SDRAM offers the larger storage capacity needed for handling extensive datasets. Together, these memory types contribute to the overall performance and effectiveness of the system, enabling successful execution of the project's objectives.

2.1.7. Phase-Locked Loop (PLL)

A Phase-Locked Loop clock is a critical component in modern electronic systems, particularly in memory technologies. It is a control system that generates a clock signal that is synchronized with a reference clock signal, ensuring that the output clock maintains a consistent phase relationship with the input clock. PLLs are widely used in various applications, including data communication, signal processing, and memory systems, due to their ability to optimize performance, enhance synchronization, manage power efficiently, and improve reliability [8].

The primary function of a PLL clock is to generate a stable output clock signal that is phase-aligned with the reference clock. In memory systems, this synchronization is crucial for ensuring that data is read from and written to memory at the correct timing intervals. The PLL adjusts the output clock frequency to match the required operational frequency of the memory devices, such as SDRAM or DDR (Double Data Rate) memory.

PLLs can multiply the frequency of the input clock signal, allowing memory systems to operate at higher frequencies than the base system clock. This capability is essential for meeting the increasing performance demands of modern applications, where higher data rates are necessary for efficient memory operations.

One of the significant advantages of using a PLL clock is its ability to reduce clock jitter, which can adversely affect the timing and reliability of data transfers. By providing a clean and stable clock signal, the PLL helps ensure that the memory operates reliably and efficiently, minimizing the risk of data corruption.

PLLs can dynamically adjust the output clock frequency based on the operating conditions and requirements of the system. This adaptability is crucial in environments where power consumption and performance need to be balanced, allowing the memory to operate efficiently under varying conditions.

Significance of PLL Clock in Memory Systems

1. **Performance Optimization:** The PLL clock is vital for optimizing the performance of memory systems. By providing a high-frequency clock signal, the PLL enables faster data access and improved throughput. This is particularly important for applications requiring high-speed memory operations, such as video processing, gaming, and data-intensive computing.
2. **Synchronization:** Synchronization of the memory devices with the system clock is critical for ensuring accurate data transfers. The PLL ensures that the memory operates in harmony with the rest of the system, preventing timing issues that could lead to data corruption or loss. This synchronization is especially important in multi-channel memory systems, where precise timing is essential for maintaining data integrity.
3. **Power Management:** The ability of the PLL to adjust the clock frequency dynamically allows for better power management in memory systems. By reducing the clock frequency during periods of low activity, the system can conserve power, which is particularly important in battery-operated devices and energy-efficient applications. This feature helps extend battery life and reduce heat generation in electronic devices.
4. **Reliability:** A stable and low-jitter clock signal is essential for the reliable operation of memory systems. The PLL's ability to minimize jitter contributes to the overall stability and reliability of the memory system, reducing the likelihood of errors during data transfers. This reliability is crucial in applications where data integrity is paramount, such as in financial transactions, medical devices, and critical infrastructure systems.

The PLL clock plays a crucial role in modern memory systems by optimizing performance, ensuring synchronization, managing power efficiently, and enhancing reliability. Its ability to generate stable, high-frequency clock signals that are phase-aligned with reference clocks is essential for meeting the demands of high-speed data access and maintaining data integrity. As memory technologies continue to evolve and demand higher performance, the importance of PLL clocks in optimizing memory operations will remain paramount. Understanding their functionality and significance is essential for designers and engineers working with contemporary memory technologies.

2.1.8. JTAG interface

The Joint Test Action Group (JTAG) interface is a standardized protocol used for testing and programming digital devices, particularly in the context of hardware design and testing processes. Originally developed for testing printed circuit boards (PCBs), JTAG has evolved into a crucial tool for debugging, programming, and verifying complex digital systems, including Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) [11].

In the context of FPGAs, JTAG is essential for programming the device with the necessary configuration data. During the development phase, designers can use JTAG to load and test different configurations, making it easier to iterate on design changes. Additionally, JTAG allows for real-time debugging of the implemented logic, which is crucial for ensuring the correct functionality of the design. For ASICs, JTAG plays a vital role in the testing and validation process. The boundary scan feature allows engineers to test the interconnections between multiple chips on a PCB, ensuring that the ASIC functions correctly in its intended environment. This capability is particularly important for high-density designs where physical access to pins may be limited. JTAG provides a powerful debugging interface that allows designers to monitor and control the internal state of a device. This capability is invaluable for identifying and resolving issues that may arise during the development process. By accessing internal registers and memory, designers can gain insights into the operation of their designs and make necessary adjustments. JTAG is widely used in manufacturing testing to verify that devices are functioning correctly before they are shipped to customers. The ability to perform boundary scan tests and in-system programming helps ensure that any defects are identified and addressed early in the production process. The standardized nature of JTAG makes it easy to integrate into existing design and testing workflows. Many development tools and environments support JTAG, allowing designers to utilize its capabilities without extensive additional training or setup.

The JTAG interface is a powerful and versatile tool in the realm of hardware design and testing, particularly for digital systems such as FPGAs and ASICs. Its capabilities for boundary scan testing, in-system programming, and real-time debugging make it an essential component of the

development process. By facilitating efficient testing and programming, JTAG helps ensure the reliability and functionality of complex digital designs, ultimately contributing to the success of hardware projects.

2.2. Development Environments

2.2.1. Quartus Prime Software

Quartus Prime is a comprehensive development software suite developed by Intel (formerly Altera) for designing and implementing digital circuits on FPGAs (Field-Programmable Gate Arrays) and CPLDs (Complex Programmable Logic Devices). It provides a complete environment for hardware design, encompassing various tools for design entry, synthesis, simulation, and programming of programmable logic devices. Quartus Prime supports a wide range of Intel FPGA families, including the Cyclone, Arria, and Stratix series [13].

The features of Quartus Prime :

1. **Design Entry:** Quartus Prime offers multiple design entry methods, including schematic capture, hardware description languages (HDLs) such as VHDL and Verilog, and graphical design entry. This flexibility allows designers to choose the method that best suits their workflow and project requirements.
2. **Synthesis:** The software includes powerful synthesis tools that convert high-level design descriptions into gate-level representations suitable for implementation on FPGAs. The synthesis process optimizes the design for performance, area, and power consumption.
3. **Simulation and Verification:** Quartus Prime provides integrated simulation tools that enable designers to verify the functionality of their designs before programming the hardware. This includes support for functional simulation, timing analysis, and debugging, ensuring that designs operate as intended.
4. **Programming and Configuration:** The software facilitates the programming and configuration of FPGAs and CPLDs. It generates the necessary programming files and supports various programming methods, including JTAG and passive serial programming.
5. **Timing Analysis:** Quartus Prime includes timing analysis tools that help designers ensure that their designs meet timing requirements. This feature is crucial for high-speed applications where timing violations can lead to functional errors.
6. **Integration with Other Tools:** The Quartus Prime environment can be integrated with other development tools and third-party software, enhancing its capabilities and allowing for a more streamlined design process.

Quartus Prime is used for a variety of purposes in the field of digital design and FPGA development:

1. **FPGA Design and Implementation:** Quartus Prime is primarily used for designing and implementing digital circuits on FPGAs. Its comprehensive toolset enables designers to create complex logic circuits, signal processing algorithms, and control systems efficiently.
2. **Prototyping and Development:** The software is widely used in research and development environments for prototyping new ideas and concepts. Designers can quickly iterate on their designs, test them in simulation, and implement them on hardware, facilitating rapid development cycles.
3. **Educational Purposes:** Quartus Prime is often used in academic settings for teaching digital design concepts and FPGA programming. Its user-friendly interface and extensive documentation make it accessible for students learning about programmable logic devices.
4. **Embedded Systems Development:** The software supports the development of embedded systems that require custom hardware solutions. Designers can implement specific algorithms and control logic tailored to their application needs, enhancing system performance and efficiency.
5. **Signal Processing Applications:** Quartus Prime is commonly used in applications involving digital signal processing (DSP), where high-speed data processing and real-time performance are essential. The software's capabilities allow for the implementation of complex DSP algorithms on FPGAs.

In summary, Quartus Prime is a powerful and versatile development software suite used for designing, implementing, and programming digital circuits on FPGAs and CPLDs. Its comprehensive features, including design entry, synthesis, simulation, and programming, make it an essential tool for engineers, researchers, and educators in the field of digital design. Whether for prototyping, embedded systems development, or educational purposes, Quartus Prime plays a crucial role in enabling the effective implementation of custom hardware solutions.

2.2.2. ModelSim Software

ModelSim is a powerful simulation and debugging tool developed by Mentor Graphics, now part of Siemens EDA. It is widely used in the field of electronic design automation (EDA) for simulating digital designs described in hardware description languages (HDLs) such as VHDL and Verilog. ModelSim provides a comprehensive environment for verifying the functionality of digital circuits, making it an essential tool for engineers and designers working on FPGA and ASIC projects [14].

The features of ModelSim:

1. **Multi-Language Support:** ModelSim supports multiple hardware description languages, including VHDL, Verilog, and SystemVerilog. This versatility allows designers to work with various projects and collaborate with teams using different languages, enhancing its utility in diverse design environments.
2. **Advanced Simulation Capabilities:** The tool offers advanced simulation features, including event-driven simulation, which efficiently manages the execution of simulations based on changes in signal states. This capability allows for faster simulation times, particularly in complex designs.
3. **Waveform Viewer:** ModelSim includes a powerful waveform viewer that enables designers to visualize signal changes over time. This feature is crucial for debugging and analyzing the behaviour of digital circuits, as it allows users to observe the interactions between different signals and components.
4. **Debugging Tools:** The software provides a suite of debugging tools, including breakpoints, watchpoints, and step-through execution. These tools help designers identify and resolve issues in their designs by allowing them to monitor specific signals and control the simulation flow.
5. **Testbench Generation:** ModelSim facilitates the creation of testbenches, which are essential for verifying the functionality of designs. Designers can easily create and manage testbenches to simulate various scenarios and ensure that their designs meet the required specifications.
6. **Integration with Other Tools:** ModelSim can be integrated with other EDA tools and environments, such as synthesis and implementation tools. This integration streamlines the design flow, allowing for a more efficient development process from simulation to hardware implementation.
7. **Support for Mixed-Signal Simulation:** In addition to digital simulation, ModelSim supports mixed-signal simulation, allowing designers to simulate both analog and digital components within the same environment. This capability is particularly valuable in designs that involve both types of signals, such as RF and mixed-signal circuits.
8. **User-Friendly Interface:** ModelSim features an intuitive user interface that simplifies navigation and operation. The graphical interface, combined with command-line capabilities, provides flexibility for users with varying preferences and expertise levels.

ModelSim Applications :

1. **FPGA and ASIC Design Verification:** ModelSim is extensively used in the verification of FPGA and ASIC designs, ensuring that the implemented logic functions as intended before

hardware fabrication. This verification process is critical for reducing errors and improving design reliability.

2. **Educational Use:** The tool is also utilized in academic settings for teaching digital design concepts and HDL programming. Its comprehensive features and user-friendly interface make it an effective resource for students learning about hardware design and simulation.
3. **System-Level Design:** ModelSim is employed in system-level design and verification, where complex interactions between various components need to be analyzed. The ability to simulate large designs and visualize signal behaviour is essential for ensuring system integrity.

ModelSim is a robust simulation and debugging tool that plays a vital role in the electronic design automation landscape. Its multi-language support, advanced simulation capabilities, and comprehensive debugging tools make it an invaluable resource for engineers and designers working on digital circuits. By facilitating thorough verification and analysis of designs, ModelSim helps ensure the reliability and functionality of FPGA and ASIC implementations, ultimately contributing to the success of electronic projects.

2.2.3. Qsys

Qsys is a system integration tool developed by Intel (formerly Altera) that is part of the Quartus Prime design software suite. It is designed to simplify the process of creating complex systems on FPGAs by providing a graphical interface for integrating various components, such as processors, memory interfaces, peripherals, and custom hardware blocks. Qsys enables designers to efficiently create, configure, and manage system-level designs, facilitating rapid development and prototyping of embedded systems [15].

The features of Qsys

1. **Graphical System Design:** Qsys provides a user-friendly graphical interface that allows designers to visually connect different components in a system. This graphical representation simplifies the design process, making it easier to understand and manage complex interconnections.
2. **Component Integration:** Qsys supports the integration of a wide range of components, including Intel's Nios II soft processor, memory blocks, peripherals (such as UARTs, timers, and GPIO), and custom logic blocks. Designers can easily add and configure these components to meet their specific application requirements.
3. **Automatic Connection Generation:** The tool automatically generates the necessary interconnect logic and protocols required for communication between components. This

feature reduces the manual effort involved in wiring components together and minimizes the risk of errors in the design.

4. **Parameterization:** Qsys allows for parameterization of components, enabling designers to customize settings such as data widths, clock frequencies, and memory sizes. This flexibility ensures that the integrated system can be tailored to meet the specific needs of the application.
5. **System-Level Simulation:** Qsys supports system-level simulation, allowing designers to verify the functionality of the integrated system before implementation. This capability is essential for identifying and resolving potential issues early in the design process.
6. **Integration with Other Tools:** Qsys is designed to work seamlessly with other tools in the Quartus Prime environment, such as the Quartus Compiler and the Nios II Software Build Tools (SBT). This integration streamlines the overall design flow, from system integration to software development.

The applications of Qsys :

1. **Embedded Systems Development:** Qsys is widely used in the development of embedded systems that require custom hardware solutions. By integrating processors, memory, and peripherals, designers can create tailored systems that meet specific application requirements, such as industrial control, automotive systems, and consumer electronics.
2. **Prototyping and Rapid Development:** The graphical nature of Qsys allows for rapid prototyping of complex systems. Designers can quickly assemble and modify system components, facilitating iterative development and testing. This capability is particularly valuable in research and development environments where time-to-market is critical.
3. **Digital Signal Processing (DSP):** Qsys is commonly used in applications involving digital signal processing, where high-speed data processing and real-time performance are essential. By integrating DSP algorithms with hardware accelerators, designers can achieve efficient implementations of complex signal processing tasks.
4. **Custom Hardware Solutions:** Qsys enables the creation of custom hardware solutions that leverage the unique capabilities of FPGAs. Designers can implement specialized algorithms or processing functions that are not available in off-the-shelf components, providing a competitive advantage in various applications.
5. **Education and Training:** Qsys is also utilized in academic settings for teaching digital design concepts and FPGA programming. Its intuitive graphical interface makes it accessible for students learning about system integration and hardware design, enhancing their understanding of complex systems.

In summary, Qsys is a powerful system integration tool that simplifies the process of designing and implementing complex systems on FPGAs. Its graphical interface, component integration capabilities, and support for parameterization and simulation make it an essential tool for engineers and designers in various fields, including embedded systems development, digital signal processing, and custom hardware solutions. By facilitating rapid prototyping and providing a streamlined design flow, Qsys plays a crucial role in enabling the effective implementation of advanced electronic systems.

2.2.4. Hardware Description Language

Hardware Description Language (HDL) is a specialized programming language used to model, design, and simulate electronic systems, particularly digital circuits. HDLs allow engineers and designers to describe the behaviour and structure of hardware components in a way that can be synthesized into physical hardware, such as Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). The power of HDL lies in its ability to provide a high-level abstraction for hardware design, enabling complex systems to be described succinctly and effectively.

HDLs provide a level of abstraction that allows designers to focus on the functionality of the hardware rather than the low-level implementation details. This abstraction facilitates easier design, modification, and understanding of complex systems.

HDLs enable the simulation of hardware designs before they are physically implemented. This capability allows designers to verify the functionality of their designs, identify potential issues, and optimize performance without the need for costly prototypes.

HDL designs can be modular and reusable, allowing components to be easily integrated into different projects. This reusability accelerates the design process and reduces development time.

HDLs can be synthesized into actual hardware using synthesis tools. This means that designs described in HDL can be translated into gate-level representations that can be implemented on FPGAs or ASICs.

HDLs inherently support parallelism, reflecting the concurrent nature of hardware operations. This allows designers to model and implement systems that can perform multiple operations simultaneously, which is crucial for high-performance applications.

Verilog is one of the most widely used hardware description languages, particularly in the design and verification of digital circuits. It was developed in the 1980s and has since become a standard for HDL due to its versatility and ease of use. Verilog allows designers to describe hardware at

various levels of abstraction, from high-level behavioural descriptions to low-level gate-level representations [16].

Verilog supports behavioural modelling, allowing designers to describe how a circuit should behave without specifying the exact implementation details. This high-level description simplifies the design process and enables rapid prototyping. In addition to behavioural modelling, Verilog allows for structural modelling, where designers can specify how different components are interconnected. This feature is useful for building complex systems from smaller, reusable modules.

Verilog provides constructs for creating testbenches, which are essential for simulating and verifying the functionality of hardware designs. Testbenches allow designers to apply stimulus to their designs and observe the outputs, facilitating thorough verification.

Verilog naturally supports concurrent execution, reflecting the parallel nature of hardware. This capability allows designers to model systems that can perform multiple tasks simultaneously, which is critical for high-performance applications.

Verilog is widely supported by synthesis tools, enabling designs to be translated into gate-level representations for implementation on FPGAs and ASICs. This compatibility makes Verilog a practical choice for hardware design [17].

In the context of this project, Verilog is utilized to implement the custom instructions and combinatorial logic required for optimizing the Fast Fourier Transform (FFT) algorithm. The following aspects highlight the relevance of Verilog in this project:

1. **Efficient Design Representation:** Verilog allows for a clear and concise representation of the combinatorial logic needed for the FFT, enabling designers to focus on the functionality without getting bogged down by low-level details.
2. **Simulation and Verification:** The ability to simulate the Verilog design before implementation is crucial for verifying the correctness of the custom instructions. This simulation helps identify potential issues early in the design process, reducing the risk of errors in the final hardware.
3. **Modularity and Reusability:** Verilog's support for modular design allows the custom instructions to be developed as reusable components. This modularity facilitates easier integration and testing within the larger system.
4. **Synthesis for FPGA Implementation:** The synthesis compatibility of Verilog ensures that the designs can be easily translated into hardware that can be implemented on the Nios II processor within an FPGA. This capability is essential for achieving the desired performance improvements in the FFT algorithm.

Hardware Description Languages, particularly Verilog, are powerful tools for designing and implementing digital systems. The abstraction, simulation capabilities, reusability, and synthesis support provided by HDLs enable efficient and effective hardware design. In this project, Verilog plays a critical role in implementing the custom instructions and combinatorial logic necessary for optimizing the FFT algorithm, ultimately enhancing the performance of the Nios II processor in real-time signal processing applications.

2.2.5. Eclipse

Eclipse is a widely-used integrated development environment (IDE) primarily designed for Java development, although it supports various programming languages through the use of plugins. Originally developed by IBM, Eclipse is now maintained by the Eclipse Foundation, which oversees its ongoing development and the community surrounding it. The IDE provides a robust set of tools for software development, including code editing, debugging, and project management, making it a popular choice among developers across different domains [18].

The features of Eclipse

1. **Modular Architecture:** Eclipse is built on a modular architecture, allowing developers to extend its functionality through plugins. This flexibility enables the integration of various tools and frameworks, accommodating a wide range of programming languages and development needs.
2. **Rich Development Tools:** The IDE offers a comprehensive suite of development tools, including a powerful code editor with syntax highlighting, code completion, and refactoring capabilities. These features enhance productivity and improve code quality.
3. **Debugging Support:** Eclipse provides integrated debugging tools that allow developers to set breakpoints, inspect variables, and step through code execution. This functionality is essential for identifying and resolving issues during the development process.
4. **Version Control Integration:** The IDE supports integration with version control systems such as Git and Subversion, enabling developers to manage their code repositories directly within the environment. This integration facilitates collaboration and version management in software projects.
5. **Project Management:** Eclipse includes project management features that help developers organize their code, manage dependencies, and configure build settings. The IDE supports various build systems, including Maven and Gradle, streamlining the build process.

6. **Cross-Platform Support:** Eclipse is a cross-platform IDE, meaning it can run on various operating systems, including Windows, macOS, and Linux. This versatility allows developers to work in their preferred environments without compatibility issues.

Significance of Eclipse in Software Development

1. **Community and Ecosystem:** Eclipse has a large and active community of developers who contribute to its ecosystem by creating plugins and extensions. This community support ensures that developers have access to a wealth of resources, tools, and documentation, enhancing their development experience.
2. **Standardization:** Eclipse has become a de facto standard for Java development, particularly in enterprise environments. Many organizations rely on Eclipse for building Java applications, and its widespread adoption has led to the establishment of best practices and conventions within the community.
3. **Support for Multiple Languages:** While Eclipse is primarily known for Java development, its extensibility allows it to support numerous programming languages, including C/C++, Python, PHP, and more. This capability makes Eclipse a versatile tool for developers working in diverse programming environments.
4. **Integration with Development Frameworks:** Eclipse seamlessly integrates with popular development frameworks and tools, such as Spring, Hibernate, and Android SDK. This integration simplifies the development process and enables developers to leverage powerful frameworks to enhance their applications.
5. **Educational Use:** Eclipse is widely used in academic settings for teaching programming and software development concepts. Its user-friendly interface and extensive features provide students with a practical environment to learn and practice coding.

In summary, Eclipse is a powerful and versatile integrated development environment that plays a significant role in software development. Its modular architecture, rich set of development tools, and extensive community support make it a popular choice among developers for building applications across various programming languages. The IDE's significance in standardizing Java development, supporting multiple languages, and integrating with popular frameworks further cements its position as a valuable tool in the software development landscape. Whether for professional development or educational purposes, Eclipse continues to be an essential resource for developers worldwide.

2.2.6. Nios II C language

The Nios II C language refers to the C programming language used in conjunction with the Nios II soft processor, developed by Intel (formerly Altera). Nios II is a highly configurable and flexible processor that can be implemented on FPGAs, allowing developers to create custom hardware solutions tailored to specific application requirements. The use of C language in programming the Nios II processor provides a high-level abstraction for developing embedded applications, enabling easier code management and faster development cycles [19].

The features of Nios II C Language

1. **High-Level Abstraction:** The C language offers a high-level abstraction that simplifies the development of complex algorithms and system functionalities. This abstraction allows developers to focus on the logic of their applications without delving into low-level hardware details.
2. **Portability:** C is a widely used programming language with a strong emphasis on portability. Code written for the Nios II processor can often be adapted for use on other platforms with minimal modifications, making it easier to share and reuse code across different projects.
3. **Rich Standard Library:** The Nios II C environment provides access to a rich set of standard libraries, including functions for input/output operations, string manipulation, and mathematical computations. These libraries facilitate rapid development and reduce the need for custom implementations of common functions.
4. **Support for Embedded Systems:** The C language is well-suited for embedded systems development, providing features such as direct memory access and hardware manipulation. This capability allows developers to efficiently interface with peripherals and manage system resources.
5. **Integration with Development Tools:** Nios II C can be seamlessly integrated with development tools like Eclipse, which provides a comprehensive IDE for writing, debugging, and managing C code. The integration with Eclipse enhances the development experience by offering features such as code completion, syntax highlighting, and debugging support.

The advantages of Using C Language with Nios II :

1. **Rapid Development:** The high-level nature of C allows for faster development cycles, enabling engineers to prototype and iterate on their designs quickly.
2. **Easier Maintenance:** C code is generally easier to read and maintain compared to lower-level programming languages, which simplifies future updates and modifications.

3. **Access to Hardware Features:** The ability to manipulate hardware directly through C provides developers with the tools needed to optimize performance and resource utilization in embedded applications.
4. **Community and Resources:** The widespread use of the C language means that developers have access to a wealth of resources, libraries, and community support, which can facilitate problem-solving and knowledge sharing.

The Nios II C language is a powerful tool for developing embedded applications on the Nios II soft processor. Its high-level abstraction, portability, and rich standard library make it an ideal choice for engineers looking to create custom hardware solutions. By leveraging development tools like Eclipse, programmers can efficiently write, debug, and manage their C code, streamlining the overall development process. The combination of C programming and the Nios II processor enables the creation of flexible and efficient embedded systems tailored to specific application requirements.

3.Methodology

The proposed solution in this project focuses on the design and implementation of a custom instruction for the butterfly operation within the Decimation-In-Time Fast Fourier Transform algorithm, utilizing the NIOS II processor in an FPGA-based environment. This approach aims to optimize the computational efficiency of the FFT, which is a critical algorithm in digital signal processing applications. The DIT algorithm optimizes computational efficiency by reducing the number of arithmetic operations needed, making it well-suited for the parallel processing capabilities of FPGAs; Multiple butterfly operations can be executed simultaneously, significantly speeding up calculations. Additionally, the NIOS II processor allows for custom instruction integration, enabling the design of tailored instructions that accelerate critical operations within the DIT algorithm, further enhancing execution speed. The DIT approach is also memory efficient, as it processes data in a time-domain sequence, minimizing memory usage and effectively utilizing the on-chip memory and SDRAM available on the DE2i-150 Board. Its inherent scalability allows the implementation to adapt to various FFT lengths and complexities, making it versatile for different applications. Furthermore, the combination of the DIT algorithm and the NIOS II processor supports real-time processing capabilities, ensuring timely data analysis for applications such as telecommunications and audio processing. Lastly, the rapid prototyping and testing capabilities of the DE2i-150 Board reduce development time, allowing for quicker iterations and refinements in design, making the DIT algorithm an ideal choice for efficient FFT implementations. The strong points of this solution include:

1. **Performance Enhancement:** By offloading the butterfly operation to a custom instruction executed in hardware, we can significantly reduce execution time compared to traditional software implementations.
2. **Resource Optimization:** The custom instruction is designed to utilize FPGA resources efficiently, allowing for more complex operations to be performed within the same hardware constraints.
3. **Flexibility and Scalability:** The NIOS II processor's configurability allows for easy adaptation of the custom instruction to various DSP applications, making it a versatile solution for future developments.
4. **Real-Time Processing Capability:** The hardware acceleration provided by the custom instruction enables real-time processing of signals, which is essential for applications in various fields, including telecommunications, audio and video processing, medical imaging, and control systems.

3.1. Custom Instructions design and implementation

Before defining the system using Qsys, the first step in the design flow is to create custom instructions for the butterfly operation in the Decimation-In-Time Fast Fourier Transform algorithm. Due to the limitations of the output ports of the combinatorial logic custom instruction, the butterfly operation was split into three distinct custom instructions. This approach allows for efficient computation while adhering to the constraints of the hardware architecture.

Overview of the Butterfly Operation

In the context of the DIT FFT, the butterfly operation is used to combine two complex numbers, typically referred to as x_0 and x_1 . These numbers are derived from the input sequence and represent the values at specific indices in the FFT computation. The butterfly operation applies a specific mathematical transformation to these values, utilizing a twiddle factor to scale the inputs appropriately.

The butterfly operation can be mathematically expressed as follows:

Given two complex numbers:

- x_0 (the first input)
- x_1 (the second input)

The butterfly operation produces two outputs:

- X_0 (the sum)
- X_1 (the difference)

The equations for the butterfly operation are defined as:

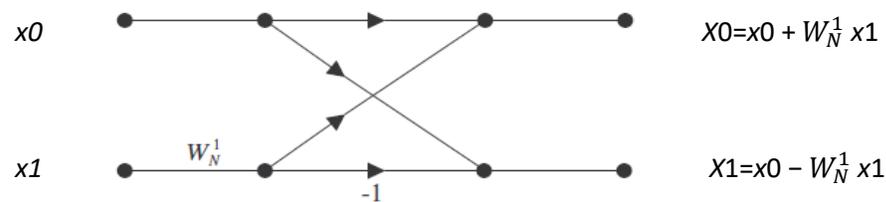


Figure 3-1: Butterfly computation for DIT radix-2 FFT

Where:

- $W_N^k = e^{-jN2\pi k}$ is the twiddle factor, which represents a complex exponential that depends on the current stage k of the FFT and the total number of points N

In this context, we consider two complex inputs, $x[0]$ and $x[1]$, represented as:

$$x[0] = a + bj$$

$$x[1] = c + dj$$

where a , b , c and d are real numbers, and j denotes the imaginary unit.

The butterfly operation combines these two complex numbers using a specific transformation that involves trigonometric functions, particularly cosine and sine. The equations for the outputs $x[0]$ and $x[1]$ are derived as follows:

1. For $X[0]$:

The output $X[0]$ is computed by adding $x[0]$ and a scaled version of $x[1]$

$$X[0] = x[0] + (x[1] e^{-j2\pi kn/N})$$

Expanding this using the definitions of $x[0]$ and $x[1]$:

$$X[0] = (a + bj) + (c + dj) * (\cos(2\pi kn/N) + j \sin(2\pi kn/N))$$

Simplifying this expression leads to:

$$X[0] = (a + c*\cos(2\pi kn/N) - d*\sin(2\pi kn/N)) + (b + c*\sin(2\pi kn/N) + d*\cos(2\pi kn/N))j$$

2. For $X[1]$:

The output $X[1]$ is computed by subtracting the scaled version of $x[1]$ from $x[0]$:

$$X[1] = x[0] - (x[1] e^{-j2\pi kn/N})$$

Again, expanding this expression gives:

$$X[1] = (a + bj) - (c + dj) * (\cos(2\pi kn/N) + j \sin(2\pi kn/N))$$

Simplifying this leads to:

$$X[1] = (a - c*\cos(2\pi kn/N) + d*\sin(2\pi kn/N)) + (-b - c*\sin(2\pi kn/N) - d*\cos(2\pi kn/N))j$$

Thus, the final equations for the outputs $X[0]$ and $X[1]$ in terms of the real and imaginary parts of the complex inputs $x[0]$ and $x[1]$ are:

$$X[0] = (a + c*\cos(2\pi kn/N) - d*\sin(2\pi kn/N)) + (b + c*\sin(2\pi kn/N) + d*\cos(2\pi kn/N))j$$

Real part

Imaginary part

$$X[1] = (a - c*\cos(2\pi kn/N) + d*\sin(2\pi kn/N)) + (-b - c*\sin(2\pi kn/N) - d*\cos(2\pi kn/N))j$$

Real part

Imaginary part

In the context of designing custom instructions for the butterfly operation in Verilog HDL, these equations serve as the foundation for the implementation. Given the limitations of the output ports of combinatorial logic custom instructions, the butterfly operation is split into three distinct custom instructions:

3.1.1. Custom Instruction for Multiplication:

The multiplier module is a fundamental building block used in the Decimation in Time Fast Fourier Transform algorithm for performing multiplication operations on signed 32-bit inputs. Specifically, this module is utilized to calculate the products of the form $c*\cos(2\pi kn/N)$, $c*\sin(2\pi kn/N)$, $d*\cos(2\pi kn/N)$ and $d*\sin(2\pi kn/N)$, where c and d are real and imaginary $x[1]$ input data. These products are essential for the butterfly operations that combine pairs of complex numbers during the FFT computation. The figure 3-2 represents the flowchart of the multiplier custom instruction.

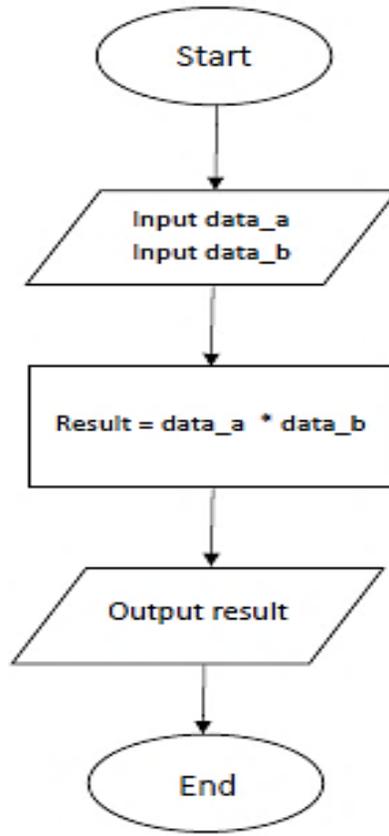


Figure 3-2 flowchart of Multiplier Custom instruction

- **Inputs:**
 - A: This 32-bit signed input represents one of the coefficients (either c or d) that will be multiplied by the respective trigonometric function (cosine or sine).
 - B: This 32-bit signed input represents the value of the cosine or sine function evaluated at the current FFT stage.
- **Output:**
 - result: This 32-bit signed output provides the product of the two input values, which represents the scaled value of the coefficient by the trigonometric function.

The multiplier module performs a straightforward multiplication operation:

- **Multiplication Operation:** The module uses the assign statement to compute the product of the two signed inputs A and B . The result is directly assigned to the output result. The synthesis tool will implement this multiplication in hardware, typically using a combination of adders and shift registers to achieve efficient computation.

These calculations are essential for the butterfly operations. The result of this custom operation is stored in variables c_cos_theta , c_sin_theta , d_sin_theta and d_cos_theta . These values are used by sending them to calculate the remainder of $calculate_X0$ and $calculate_X1$ custom instructions.

3.1.2. Custom Instruction for $X[0]$:

The $calculate_X0$ module is designed to perform a critical operation within the Decimation in Time Fast Fourier Transform algorithm. Specifically, it implements part of the butterfly operation, which is essential for efficiently combining pairs of complex numbers during the FFT computation. This module processes two 32-bit input words, extracts relevant components, and computes the resulting values that contribute to the overall FFT output. The figure 3-3 represents the flowchart of the custom instruction $calculate_X0$.

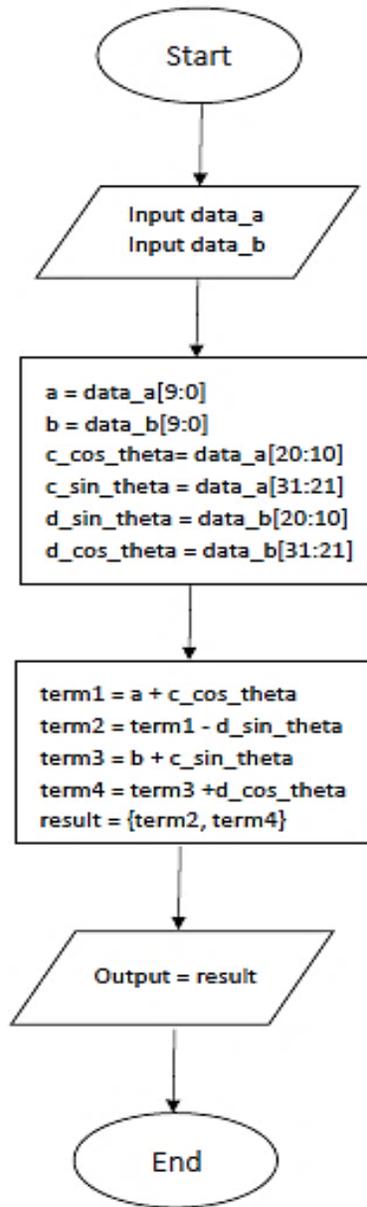


Figure 3-3 flowchart of Custom instruction Calculate X0

- **Inputs:**
 - data_a: This 32-bit input contains three components:
 - a: The first part (10 bits) represents real part of x[0] input values.
 - c_cos_theta: The second part (11 bits) represents the cosine of the angle associated with the FFT stage.

- **c_sin_theta:** The third part (11 bits) represents the sine of the angle associated with the FFT stage.
- **data_b:** This 32-bit input contains three components:
 - **b:** The first part (10 bits) represents imaginary part of $x[0]$ input value.
 - **d_sin_theta:** The second part (11 bits) represents the sine of the angle for the second input.
 - **d_cos_theta:** The third part (11 bits) represents the cosine of the angle for the second input.
- **Output:**
 - **result:** This 32-bit output combines the results of the calculations performed in the module, specifically the results of the butterfly operation.

The calculate_X0 module performs several key calculations to achieve its purpose:

- **Extraction of Components:** The module splits the input data into its respective parts using bit slicing. This allows it to access the individual components necessary for the butterfly operation.
- **Intermediate Signal Calculations:**
 - **Term Calculations:**
 - **term1:** This computes the sum of a and c_cos_theta , which is part of the butterfly operation.
 - **term2:** This subtracts d_sin_theta from $term1$, contributing to the first output of the butterfly operation.
 - **term3:** This computes the sum of b and c_sin_theta , which is necessary for the second output of the butterfly operation.
 - **term4:** This adds d_cos_theta to $term3$, finalizing the second output of the butterfly operation.
- **Result Assignment:** The final output result is constructed by concatenating $term2$ which is the real part and $term4$ which is the imaginary part. This output represents the combined results of the butterfly operation, which will be used in subsequent stages of the FFT computation.

The butterfly operation is a fundamental aspect of the DIT FFT algorithm, where pairs of complex numbers are combined to produce new values that reflect the frequency components of the input signal. The calculate_X0 module directly implements part of this operation by performing the necessary arithmetic on the components extracted from the input data.

3.1.3. Custom Instruction for X[1] :

The calculate_X1 module in the figure is designed to perform a critical operation within the context of the Decimation in Time Fast Fourier Transform algorithm. Specifically, it implements part of the butterfly operation, which is essential for efficiently combining pairs of complex numbers during the FFT computation. This module takes two 32-bit input words, processes them to extract relevant components, and computes the resulting values that contribute to the overall FFT output. The figure 3-4 represents the flowchart of the custom instruction calculate X1.

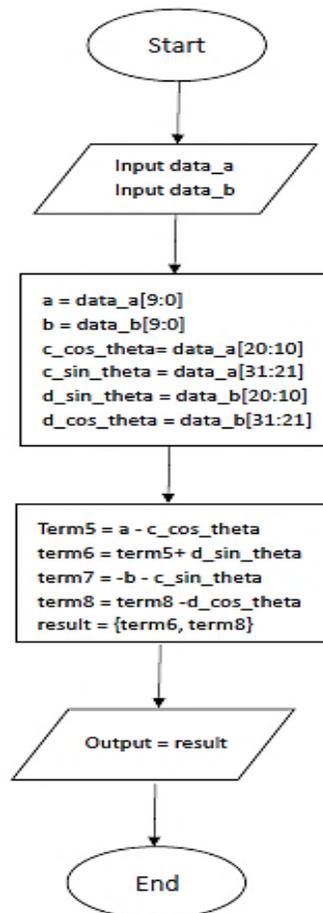


Figure 3-4 flowchart of Custom instruction Calculate X1

Inputs:

- **data_a:** This 32-bit input contains three components:
 - **a:** The first part (10 bits) represents real part of $x[0]$ input values.
 - **c_cos_theta:** The second part (11 bits) represents the cosine of the angle associated with the FFT stage.
 - **c_sin_theta:** The third part (11 bits) represents the sine of the angle associated with the FFT stage.
- **data_b:** This 32-bit input contains three components:
 - **b:** The first part (10 bits) represents imaginary part of $x[0]$ input value.
 - **d_sin_theta:** The second part (11 bits) represents the sine of the angle for the second input.
 - **d_cos_theta:** The third part (11 bits) represents the cosine of the angle for the second input.

Output:

- **result:** This 32-bit output combines the results of the calculations performed in the module, specifically the results of the butterfly operation.

The calculate_X1 module performs several key calculations to achieve its purpose:

- **Extraction of Components:** The module splits the input data into its respective parts using bit slicing. This allows it to access the individual components necessary for the butterfly operation.
- **Intermediate Signal Calculations:**
 - **Term Calculations:**
 - **term5:** This computes the difference between a and c_cos_theta , which is part of the butterfly operation.

- term6: This adds d_{\sin_theta} to term5, contributing to the first output of the butterfly operation.
- term7: This computes the negative of b and subtracts c_{\sin_theta} , which is necessary for the second output of the butterfly operation.
- term8: This subtracts d_{\cos_theta} from term7, finalizing the second output of the butterfly operation.
- **Result Assignment:** The final output result is constructed by concatenating term6 which is the real part and term8 which is the imaginary part. This output represents the combined results of the butterfly operation, which will be used in subsequent stages of the FFT computation.

The butterfly operation is a fundamental aspect of the DIT FFT algorithm, where pairs of complex numbers are combined to produce new values that reflect the frequency components of the input signal. The `calculate_X1` module directly implements part of this operation by performing the necessary arithmetic on the components extracted from the input data.

By structuring the custom instructions in this manner, we can efficiently implement the butterfly operation while adhering to the constraints of the hardware architecture. This approach not only optimizes performance but also facilitates the integration of the butterfly operation into the overall FFT computation within the NIOS II processor.

The butterfly operation is a critical aspect of the DIT FFT algorithm, enabling efficient computation of the DFT. By breaking down the operation into manageable custom instructions, we can leverage hardware acceleration to enhance the performance of FFT computations in digital signal processing applications.

3.2. Define system using Qsys

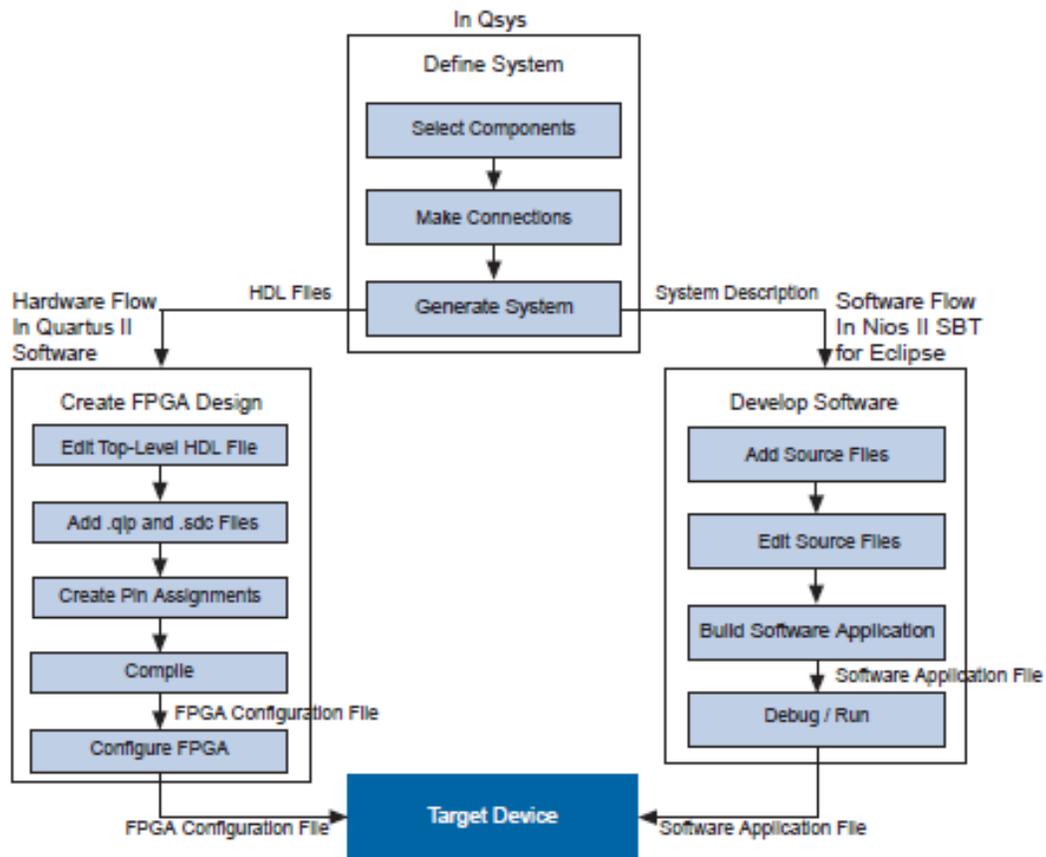


Figure 3-5 System Design Flow

The design flow for creating custom instructions for the butterfly operation in the Fast Fourier Transform shown in the figure 3-1 involves several critical steps, including defining the system using Qsys, selecting components, establishing connections, and generating the system. This section outlines the entire process in detail.

Qsys (now known as Platform Designer) is an integrated development environment provided by Intel (formerly Altera) for designing systems on FPGAs. To build the system follow these steps:

The first step involves selecting the necessary components for the system. The following components are essential for implementing the FFT algorithm:

1. **NIOS II Processor:** Select the NIOS II processor as the central processing unit.
2. **SDRAM IP:** Adding an SDRAM to interface with external SDRAM, providing additional memory resources for larger datasets.

3. **Custom Instructions:** Create a custom instruction module specifically for the butterfly operation. This module was designed using Verilog HDL and integrated into the NIOS II processor by adding the process file as in Figure 3-6 and set the ports as shown Figure 3-7 to become a custom instruction.

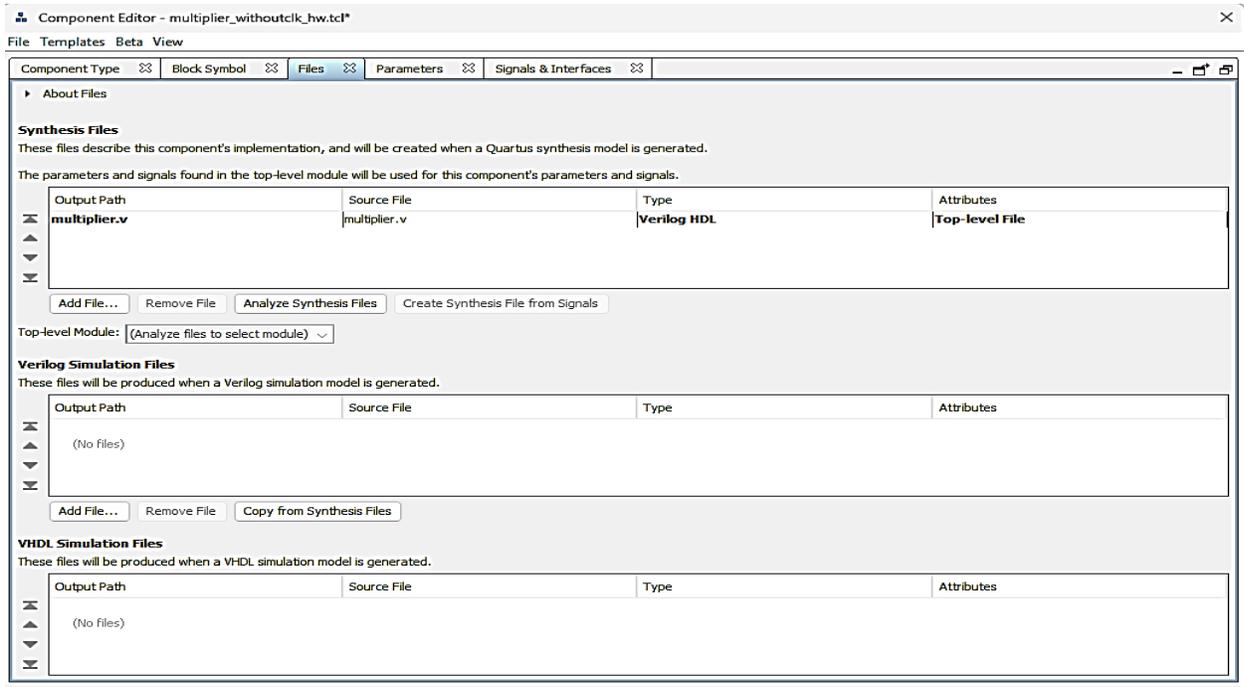


Figure 3-6: adding the custom instruction file

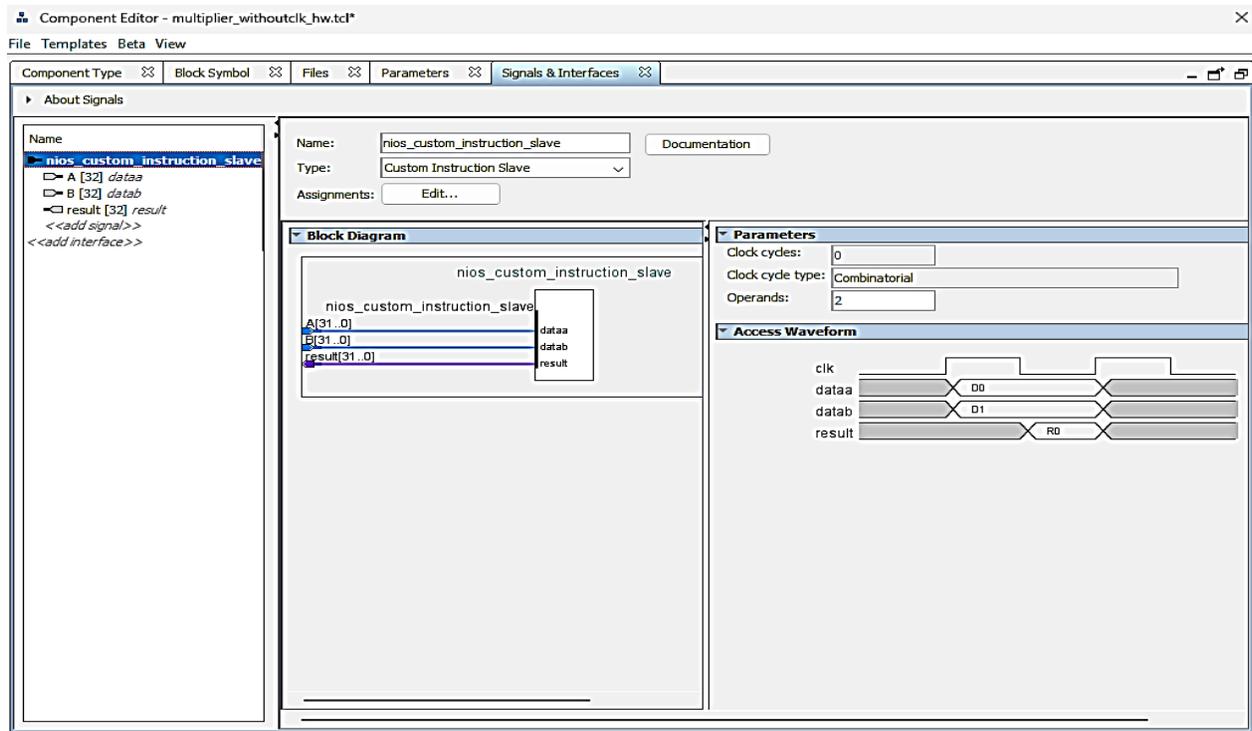


Figure 3-7: Set the custom instruction signals

4. **JTAG Interface:** Include a JTAG interface for in-system programming and debugging capabilities, allowing for real-time monitoring and modification of the design.
5. **Timer:** Add a timer component to manage execution timing and control the flow of operations during FFT processing.
6. **System and SDRAM Clocks:** Configure the system and SDRAM clocks to ensure proper timing and synchronization across the entire system.

Once the components are selected, the next step is to establish connections between them as in Figure 3-8:

1. **Connect the NIOS II Processor:** Link the NIOS II processor to the on-chip memory and SDRAM, ensuring that data can be efficiently accessed and processed.
2. **Integrate Custom Instructions:** Connect the custom instruction modules to the NIOS II processor, allowing it to be executed as part of the processor's instruction set. Then set the Opcode for each one.
3. **Connect the JTAG Interface:** Establish a connection between the JTAG interface and the NIOS II processor to facilitate programming and debugging.

- Integrate Timer:** Connect the timer to the NIOS II processor to manage execution timing for the FFT computations.
- Configure Clocks:** Ensure that the system and SDRAM clocks are properly connected to all relevant components to maintain synchronization.

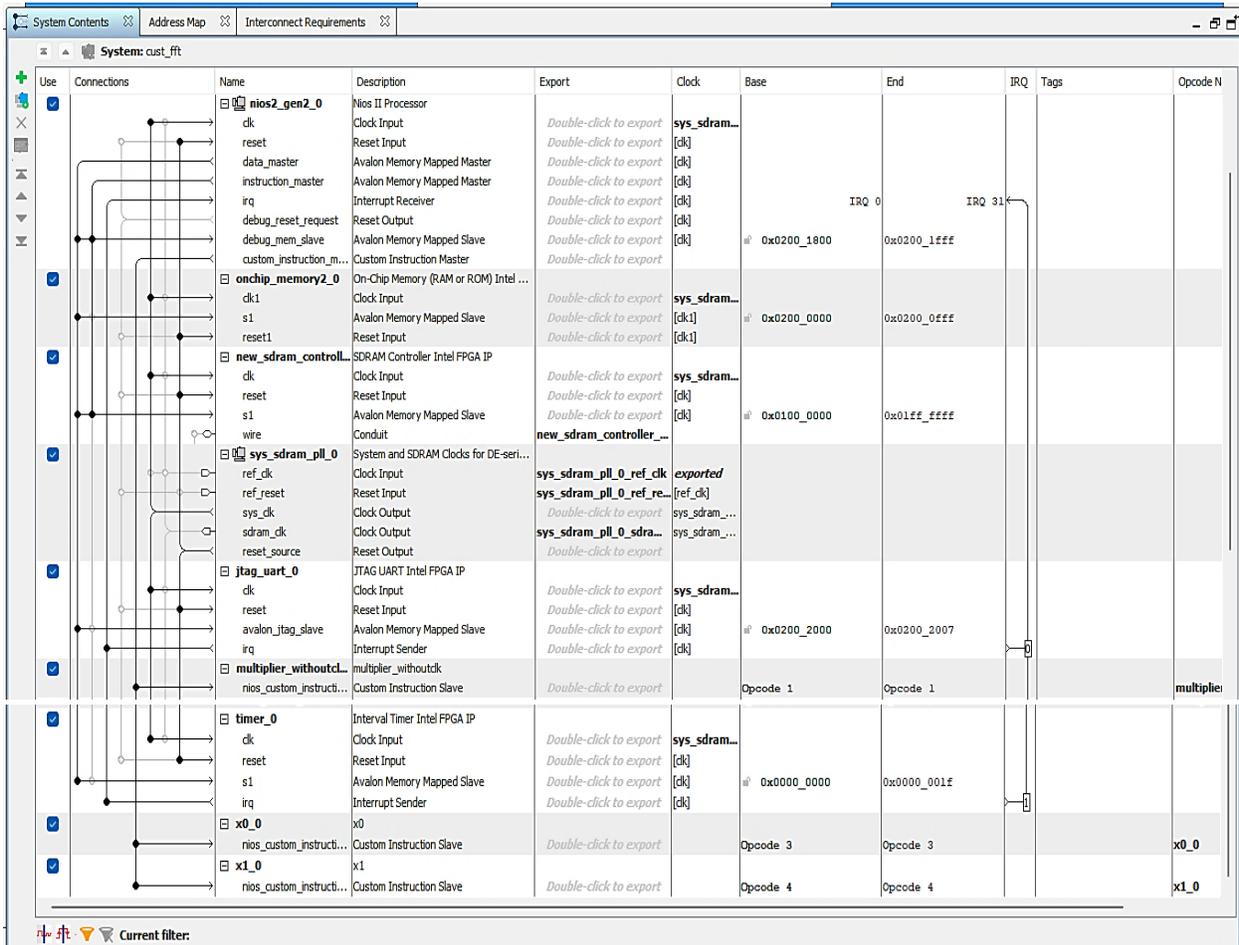


Figure 3-8: component connection in Qsys.

After establishing all connections, the final step is to generate the system:

- System Generation:** This process will compile all the components and connections into a cohesive design.
- HDL File Generation:** Upon successful generation, two key files will be created:
 - HDL Files:** These files contain the hardware description language code for the entire system, which will be used in Quartus Prime for synthesis and implementation.

- **System Description File:** This file provides a description of the system for the NIOS II Software Build Tools (SBT) for Eclipse, detailing how the software will interact with the hardware components.

3. **Exporting Files:** Ensure that the generated HDL files and system description file are correctly exported and saved in the appropriate project directory for further development.

3.3. Hardware Design Flow

After getting the HDL file from the Qsys and adding it to the project in the Quartz Prime and make it a Top-Level Entity, the next step is to do a simple programmatic conversion to get the unconnected pins in the system and connect them by filling in their data using the assignment editor as in Figure 3-9. The data is filled in based on the user manual for the board used in this project.

tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1		out new_s...dr[1]	Location	PIN_AJ7	Yes			
2		out new_s...dr[2]	Location	PIN_AG8	Yes			
3		out new_s...dr[3]	Location	PIN_AH8	Yes			
4		out new_s...dr[4]	Location	PIN_AE16	Yes			
5		out new_s...dr[5]	Location	PIN_AF16	Yes			
6		out new_s...dr[6]	Location	PIN_AE14	Yes			
7		out new_s...dr[7]	Location	PIN_AE15	Yes			
8		out new_s...dr[8]	Location	PIN_AE13	Yes			
9		out new_s...dr[9]	Location	PIN_AE12	Yes			
10		out new_s...r[10]	Location	PIN_AH6	Yes			
11		out new_s...r[11]	Location	PIN_AE11	Yes			
12		out new_s...ba[0]	Location	PIN_AH5	Yes			
13		out new_s...ba[1]	Location	PIN_AG6	Yes			
14		io new_...q[0]	Location	PIN_AD10	Yes			
15		io new_...q[1]	Location	PIN_AD9	Yes			
16		io new_...q[2]	Location	PIN_AE9	Yes			

Figure 3-9: Connect the pins using assignment editor

Then start the Full Compilation to compile the project before download it in the target FPGA device. After complete the compilation successfully, the compilation produces the .sof file that

is the file to be downloaded to the Cyclone IV GX EP4CGX150DF31C7 device in the DE2i-150 board using programmer as in Figure 3-10.

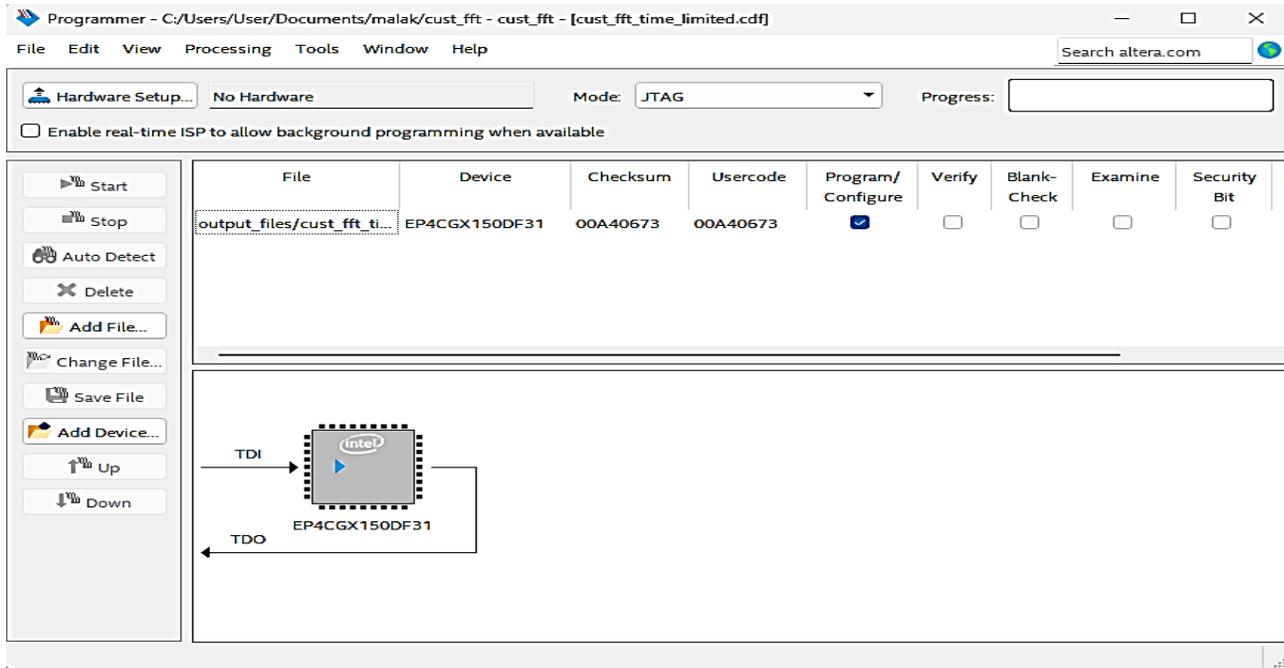


Figure 3-10: Download the .sof file to Cyclone IV GX EP4CGX150DF31C7 device.

3.4. Software Design Flow

In the software flow, the Nios II SBT for Eclipse is utilized to develop the software application that operates on the system. A new software application project is created, along with a board support package (BSP) for the project, which provides a software runtime environment tailored for the hardware system defined in the hardware flow. The software source files are added to the project, the project is configured, and the project is built. The outcome of the build process is an .elf file. The application .elf is then downloaded to the memory location expected by the Nios II processor for locating the executable program. Subsequently, the application .elf is executed by the Nios II processor.

For creating the Board Support Package (BSP) project using the Nios II Software Build Tools (SBT) for Eclipse, a systematic approach was employed. Initially, the Nios II SBT for Eclipse was started on the respective operating system.

Upon the appearance of the Workspace Launcher dialog box, the default workspace location was accepted by clicking OK Figure 3-11. The main program interface appears as shown in the Figure 3-12.

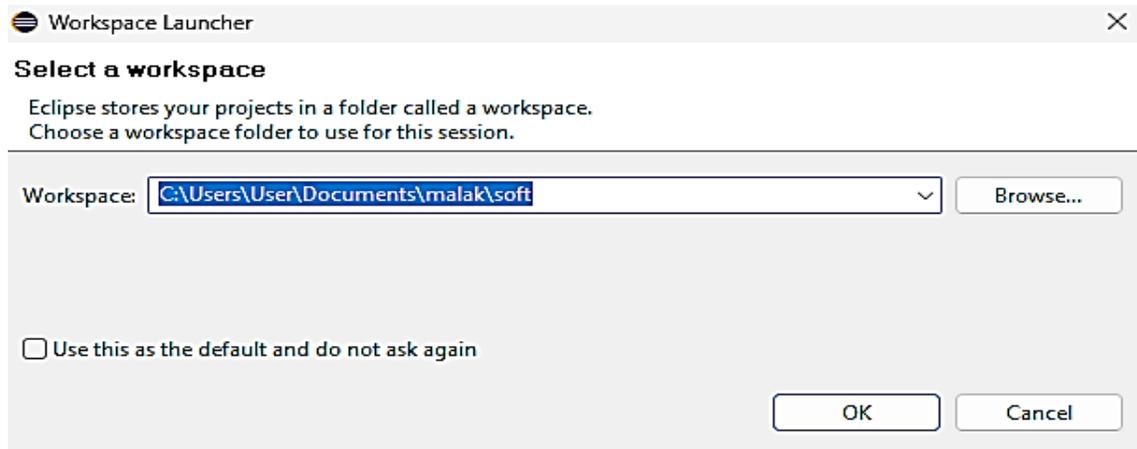


Figure 3-11: Workspace Launcher

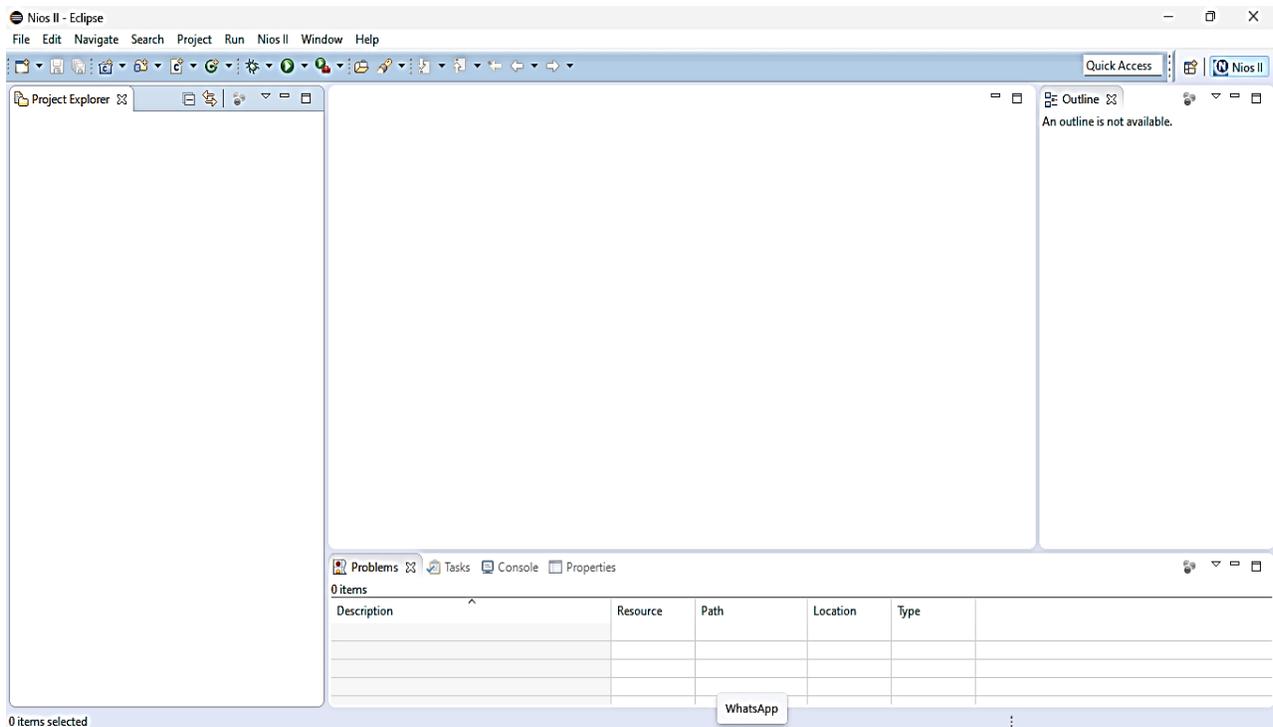


Figure 3-12: NIOS II Eclipse interface

From the NEW icon, a select wizard window appears Figure 2-14. Through it, an option is Nios II Application and BSP from Template selected.

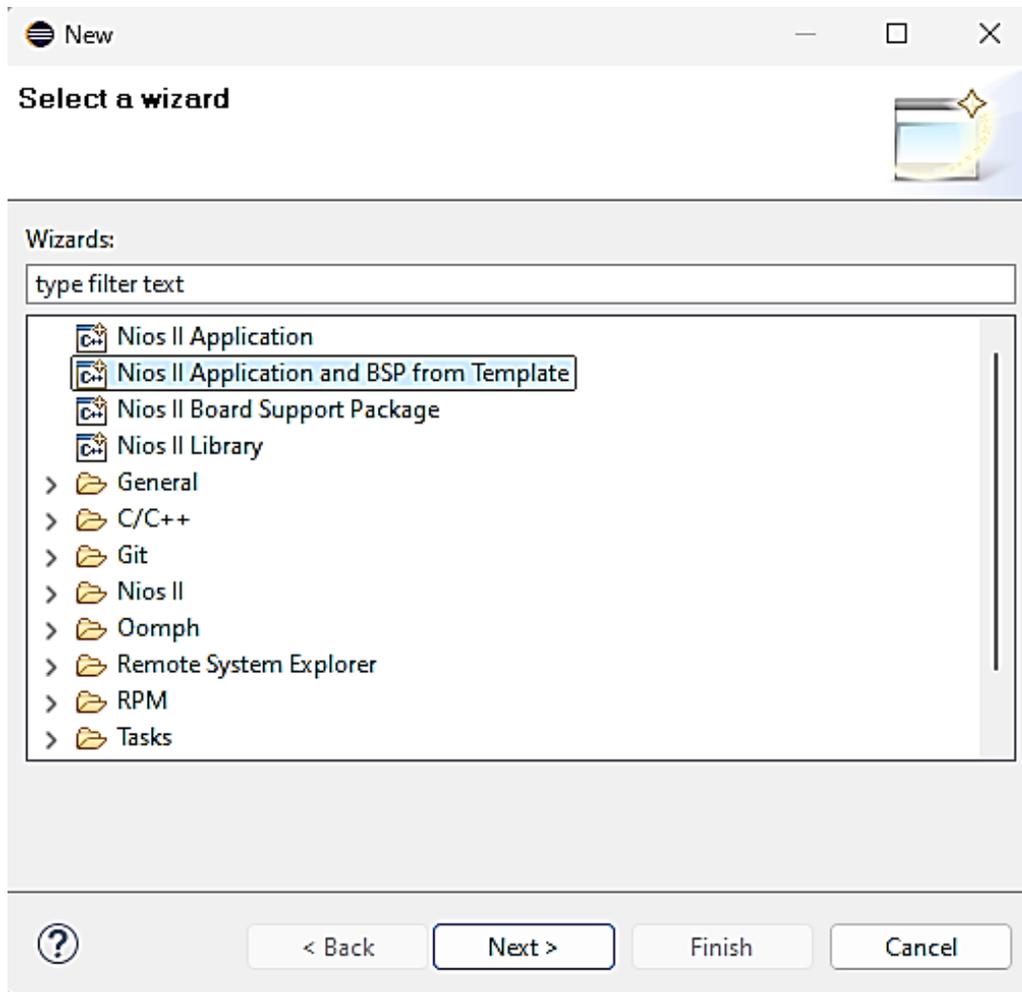


Figure 3-13: select wizard window

After confirming the option, a Nios II Application and BSP from Template window appears Figure 3.13 through which the SOPC file for the project is selected. When this file is selected, the name of the processor that was assigned through the Qsys will appear in the CPU name field, then the name for the software project is written in the project name field.

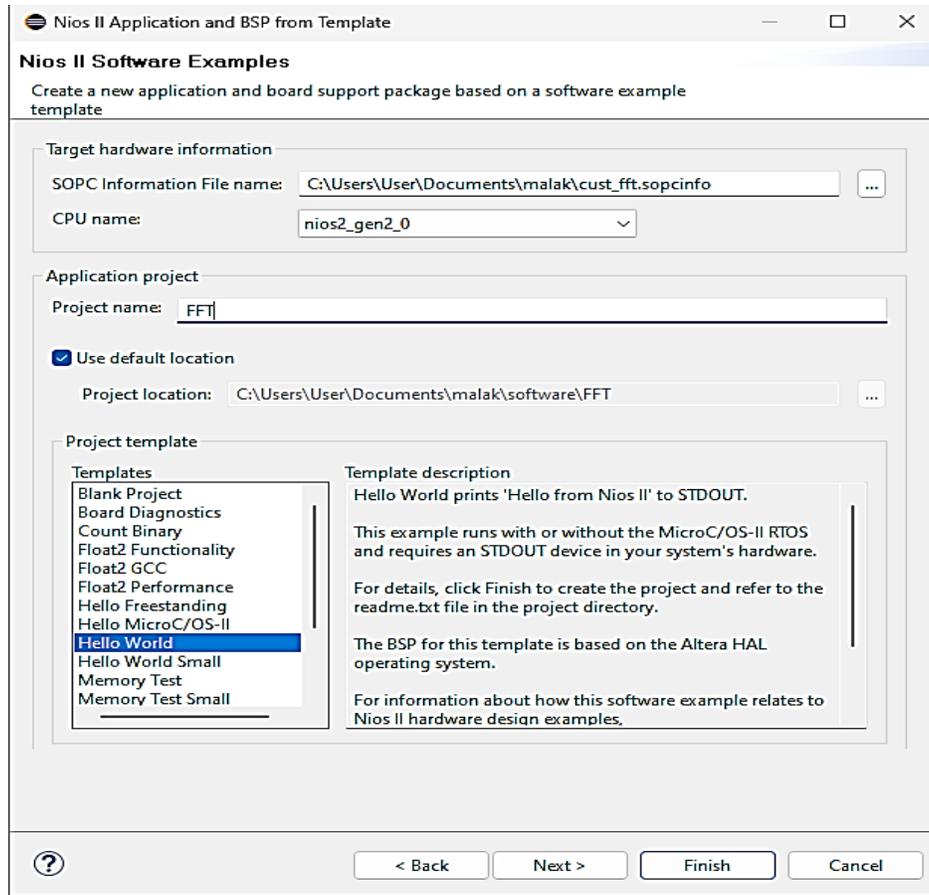


Figure 3-14: Nios II Application and BSP from Template window.

The implementation of the Fast Fourier Transform (FFT) using the Decimation in Time (DIT) algorithm on the NIOS II processor in the Appendix A be approached through two primary methods: a software-only (non-custom) execution and an execution that leverages custom instructions. This section delves into the specifics of both approaches, highlighting their design, functionality, and performance implications.

The code begins by including essential libraries that facilitate mathematical computations, memory management, and system-level operations:

- **Standard Libraries:** These include `stdio.h`, `stdlib.h`, `math.h`, and `stdint.h`, which provide functionalities for input/output operations, dynamic memory allocation, mathematical functions, and fixed-width integer types, respectively.
- **System Libraries:** `system.h` and `alt_types.h` are specific to the NIOS II architecture, providing system-level definitions and data types.

- **Performance Measurement:** The time.h headers are included to facilitate performance measurement through a hardware timer.

The implementation uses fixed-point arithmetic to enhance performance while maintaining precision:

```
11 #define FRACTIONAL_BITS 16
12 #define FIXED_POINT_SCALE (1 << FRACTIONAL_BITS)
```

The number of fractional bits is defined, allowing for the conversion between floating-point and fixed-point representations. This is crucial for optimizing the FFT calculations, especially in hardware implementations.

Conversion Functions:

```
15 // Helper functions to convert between float and fixed-point integer
16 int float_to_fixed(float f) {
17     return (int)(f * FIXED_POINT_SCALE);
18 }
19
20 float fixed_to_float(int i) {
21     return (float)i / FIXED_POINT_SCALE;
22 }
```

These helper functions convert between floating-point and fixed-point formats, enabling efficient arithmetic operations in the FFT algorithm.

The FFT is implemented using the Decimation in Time (DIT) approach. The functions `fft_custom` and `fft_software` is defined as follows:

```
void fft_custom(int* real, int* imag, int n) {
    // Variable declarations

    // Bit-reversal permutation

    // FFT calculation using DIT
}

void fft_software(int* real, int* imag, int n) {
    // Variable declarations

    // Bit-reversal permutation

    // FFT calculation using DIT
}
```

The main FFT computation is performed in stages. For each stage, twiddle factors (complex exponentials) are computed, and the butterfly operation using custom instructions in `fft_custom` and using standard arithmetic in `fft_software` :

The DIT FFT operates on a sequence of complex numbers, typically represented as two separate arrays: one for the real parts and one for the imaginary parts. The length of the input data must be a power of 2 (e.g., 256, 512, 1024, etc.), which simplifies the computation.

In C, dynamic memory allocation is often used to handle large datasets. You will need to allocate memory for the real and imaginary parts of the input data, as well as for any temporary variables used during computation. This can be done using the `malloc` function:

The first step in the DIT FFT algorithm is to rearrange the input data using a bit-reversal permutation. This step ensures that the data is organized in a manner conducive to efficient processing. The bit-reversal permutation involves the following steps:

- Calculate the number of bits required to represent the length of the input n using $\log_2(n)$.
- Loop through each index i from 0 to $n-1$ and compute the bit-reversed index j .
- If j is greater than i , swap the elements at indices i and j for both the real and imaginary arrays.

Once the input data has been rearranged, the main FFT computation begins. This involves iterating through multiple stages, where each stage combines smaller FFTs into larger ones. The steps for this computation are as follows:

- **Stage Loop:** Loop through each stage from 1 to the number of bits (i.e., $\log_2(n)$).
- **Step Size Calculation:** For each stage, calculate the step size, which is 2^{stage} , and the `half_size`, which is half of the step.
- **Butterfly Operations:** For each half-size, calculate the twiddle factors (complex exponentials) based on the current stage and butterfly index. The twiddle factors are computed using cosine and sine functions.

During each butterfly operation, the real and imaginary parts of the input data are updated based on the results of the calculations. The new values are computed as follows:

- For each index i , compute the temporary values t_real and t_imag using the Traditional instructions sets in the non-custom function and using the custom instructions in the custom function.
- Update the values at indices i and j in the real and imaginary arrays.

After completing all stages of the FFT computation, the final output will be stored in the real and imaginary arrays. These arrays represent the frequency components of the original input signal.

Main Function

The main function orchestrates the execution of the FFT algorithm. By allowing users to input the length of the FFT and the corresponding real and imaginary parts of the data. It begins by allocating memory for the real and imaginary arrays, as well as copies for a non-custom implementation. After checking for successful memory allocation, the user is prompted to enter the values for each input. The code then measures the execution time for the FFT using custom instructions, followed by the non-custom FFT implementation, calculating the elapsed time for both methods. The results of each FFT computation are printed, along with a performance comparison highlighting the execution times of the two approaches. Finally, the code ensures proper memory management by freeing the allocated memory for all arrays, preventing memory leaks and maintaining efficient resource usage. This structure emphasizes the importance of performance optimization in digital signal processing applications.

Performance Measurement: The execution time for both the custom instruction-based FFT and the non-custom FFT are measured using the `clock()` function.

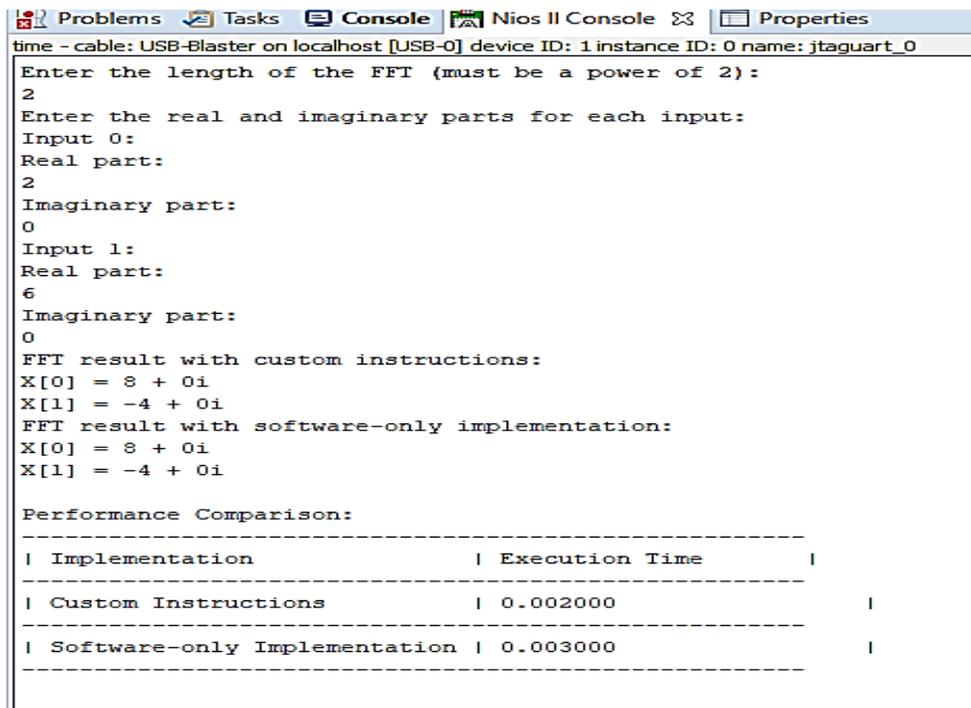
4.Results

This chapter presents the results obtained from the implementation of the Fast Fourier Transform algorithm using custom instructions on the NIOS II Embedded Processor. The primary objective of this study is to evaluate the performance improvements achieved through hardware acceleration compared to a traditional non-custom implementation. The results are organized to highlight key performance metrics, including execution time, while providing a comparative analysis of both approaches.

The experiments were conducted on a NIOS II processor implemented on a DE2i-150 FPGA platform. The development environment utilized includes Quartus Prime for hardware design and NIOS II Software Build Tools for C programming. The processor was configured with custom instructions specifically designed to enhance the FFT computation.

4.1 Results Presentation

The results of the Fast Fourier Transform computations shown in Figure 4-1 performed using both custom instructions and a non-custom implementation. The input data consisted of two complex numbers with specified real and imaginary parts. The FFT algorithm was executed to analyse the frequency components of the input signal.



```
time - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtaguart_0
Enter the length of the FFT (must be a power of 2):
2
Enter the real and imaginary parts for each input:
Input 0:
Real part:
2
Imaginary part:
0
Input 1:
Real part:
6
Imaginary part:
0
FFT result with custom instructions:
X[0] = 8 + 0i
X[1] = -4 + 0i
FFT result with software-only implementation:
X[0] = 8 + 0i
X[1] = -4 + 0i

Performance Comparison:
-----
| Implementation                | Execution Time          |
-----|-----|
| Custom Instructions            | 0.002000                |
-----|-----|
| Software-only Implementation  | 0.003000                |
-----|-----|
```

Figure 4-1 results of FFT computation

The FFT results obtained from both the custom instructions and the software-only implementation are identical, indicating that both methods successfully computed the FFT of the input data. The results can be interpreted as follows:

- **Frequency Component X[0]:** The value $8+0i$ represents the DC component (zero frequency) of the input signal, which is the sum of the input values. This is expected, as the sum of the real parts (2 + 6) yields 8, and the imaginary parts are both zero.
- **Frequency Component X[1]:** The value $-4+0i$ represents the first harmonic component of the signal. This result can be attributed to the nature of the input data, where the second input contributes negatively to the first harmonic due to its phase relationship in the context of the FFT.

The FFT computations for the given inputs demonstrate the effectiveness of both the custom instruction-based and non-custom implementations in calculating the frequency components of a signal. The identical results from both methods validate the correctness of the FFT algorithm and highlight the performance optimization achieved through custom instructions.

The Figure 4-2 shown the simulation of the FFT custom instruction.



Figure 4-2 simulation waveform of FFT custom instruction

The execution times for both implementations and the corresponding speed increase and percentage of it summarized in Table 1 below.

The increase in speed as in the equation (1) and speed up percentage as in the equation (2) due to custom implementation of the butterfly processor is given by:

$$\text{Speed Increase} = \frac{\text{Execution time for non-custom implementation}}{\text{Execution time for Custom implementation}} \quad (1)$$

$$\text{Speed up \%} = \frac{\text{Execution time for non-custom} - \text{Execution time for Custom}}{\text{Execution time for non-Custom}} \times 100 \% \quad (2)$$

Table 1: Execution Times and Speed Increase for FFT Implementations

Length Of FFT	Execution time for Non-Custom Implementation	Execution time for Custom instruction Implementation	Speed increase	Speed up %
128	0.099 s	0.058 s	1.707	41.4%
256	0.210 s	0.122 s	1.72	41.9%
512	0.333 s	0.142 s	2.34	57.4%
1024	1.004 s	0.533 s	1.88	46.9%
4096	4.523 s	2.210 s	2.05	51.1%

Results Analysis

1. Execution Time Comparison:

- The execution time for the non-custom implementation increased with the length of the FFT, reflecting the inherent computational complexity of the algorithm. For instance, the execution time rises from 0.099 seconds for an FFT length of 128 to 4.523 seconds for an FFT length of 4096.
- Conversely, the custom instruction implementation demonstrates a more moderate increase in execution time, from 0.058 seconds for an FFT length of 128 to 2.210 seconds for an FFT length of 4096. This indicates that the custom instructions effectively reduce the computational burden associated with larger FFT sizes.

2. Speed Increase:

- The speed increase, calculated as the ratio of execution times for the software-only implementation to the custom instruction implementation, shows significant improvements across all tested FFT lengths. The highest speed increase of 2.340 is observed for the FFT length of 512, indicating that the custom instruction implementation is more than twice faster the non-custom version for this specific length.
- The speed increase remains consistently above 1.7 for all lengths, with values of 1.707 for 128, 1.720 for 256, and 1.880 for 1024. The speed increase for the 4096 length is slightly lower at 2.050, but still demonstrates a substantial performance enhancement.
- The custom instruction implementation demonstrated a 57.4% reduction in execution time compared to the non-custom implementation.

3. Implications for Real-Time Processing:

- The results underscore the importance of optimizing FFT computations, particularly in applications requiring real-time processing. The ability to execute FFTs significantly faster through custom instructions can enhance the performance of systems in telecommunications, audio processing, and other domains where rapid signal analysis is critical.

- The consistent speed increases observed across various FFT lengths indicate that leveraging custom instructions can lead to more efficient resource utilization and improved overall system performance.

The Power Analyzer Status report shown in Figure 4-1 for the Quartus Prime Version 18.1.0 Build 625 provides critical insights into the thermal power dissipation characteristics of the design specified as "cust_fft" within the Cyclone IV GX family. This analysis will focus on the thermal power dissipation values and the associated estimation confidence levels.

Power Analyzer Summary	
 <<Filter>>	
Power Analyzer Status	Successful - Sun Aug 11 22:57:50 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Standard Edition
Revision Name	cust_fft
Top-level Entity Name	cust_fft
Family	Cyclone IV GX
Device	EP4CGX150DF31C7
Power Models	Final
Total Thermal Power Dissipation	160.04 mW
Core Dynamic Thermal Power Dissipation	1.30 mW
Core Static Thermal Power Dissipation	125.93 mW
I/O Thermal Power Dissipation	32.80 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 4-3power analyzer summary

Total Thermal Power Dissipation: The report indicates a total thermal power dissipation of **160.04 mW**. This value represents the overall power consumed by the device during operation, encompassing dynamic and static components.

Core Dynamic Thermal Power Dissipation: The dynamic thermal power dissipation for the core is recorded at **1.30 mW**. This figure reflects the power consumed by the device during active switching operations. The relatively low value suggests that the design may not be heavily utilized or that the toggle rates are minimal.

Core Static Thermal Power Dissipation: The core static thermal power dissipation is noted as **125.93 mW**. This portion of the power dissipation is attributed to leakage currents and other static power components when the device is not actively switching. The significant contribution

of static power dissipation indicates that a considerable amount of power is consumed even in idle states, which is a common characteristic in FPGA designs.

I/O Thermal Power Dissipation: The I/O thermal power dissipation is reported at **32.80 mW**. This value accounts for the power consumed by the input/output pins during operation. The I/O power dissipation is critical, especially in designs with high I/O activity, as it can significantly impact the overall thermal profile of the device.

The Figure 4-4 illustrates the Register Transfer Level (RTL) representation of the optimized Fast Fourier Transform (FFT) implementation utilizing custom instructions on the Nios II processor. The RTL viewer provides a detailed schematic of the hardware architecture.

5. Conclusion and Future Work

This project has successfully demonstrated the implementation and optimization of the Fast Fourier Transform (FFT) algorithm using a Nios II processor on the DE2i-150 FPGA platform for design custom instruction. The primary focus was on leveraging custom instructions to enhance the performance of FFT computations, which are critical in various real-time digital signal processing applications.

The results indicate that the custom instruction implementation significantly reduces execution times compared to the non-custom version. The highest observed speed increase of 57.4% for an FFT length of 512 exemplifies the effectiveness of custom instructions in accelerating FFT computations. This optimization is crucial for applications requiring rapid signal analysis, such as telecommunications and audio processing, where timely responses are essential.

The ability to execute FFTs more efficiently through custom instructions underscores the importance of performance optimization in real-time processing environments. The consistent speed increases across various FFT lengths suggest that utilizing custom instructions not only enhances computational speed but also improves resource utilization within the FPGA. This capability is vital for applications that demand high throughput and low latency, ensuring that systems can process data in real time without bottlenecks.

The insights gained from this project not only validate the effectiveness of the implemented techniques but also serve as a foundation for future research and development efforts aimed at further enhancing the performance and efficiency of digital signal processing algorithms in FPGA environments.

Future research in optimizing signal processing algorithms could focus on several promising areas, including the development of advanced custom instructions specifically tailored for various signal processing algorithms beyond the Fast Fourier Transform (FFT). By analyzing performance bottlenecks in algorithms such as filtering, convolution, and wavelet transforms, researchers can create custom instructions that significantly enhance operational efficiency and performance across a broader range of applications. Additionally, as machine learning continues to gain traction in signal processing, integrating FFT computations with machine learning algorithms presents an exciting opportunity for future exploration. This integration could involve

optimizing FFT for preprocessing tasks in machine learning models, such as feature extraction from time-series data, which may improve performance in critical areas like speech recognition, image processing, and biomedical signal analysis. Furthermore, while this project utilized the DE2i-150 FPGA platform, future work could investigate other FPGA platforms with diverse architectures and capabilities. By comparing performance metrics across different FPGA families, researchers can identify the most suitable platforms for specific applications and optimize custom instructions accordingly. This exploration could also encompass newer FPGA technologies that promise enhanced performance and power efficiency, thereby broadening the scope of potential applications in real-time signal processing.

In summary, this project highlights the substantial benefits of optimizing FFT computations through custom instructions on the Nios II processor, demonstrating the successful execution of the FFT algorithm alongside an analysis of performance improvements and thermal power dissipation. This success underscores the viability of utilizing FPGAs for real-time digital signal processing tasks, contributing to the ongoing development of efficient hardware solutions tailored to specific application requirements and paving the way for advancements in various fields, including telecommunications, audio processing, and embedded systems. Furthermore, the effective implementation and optimization of the FFT algorithm using custom instructions on the Nios II processor and DE2i-150 FPGA platform opens up numerous avenues for future work and research. By exploring advanced custom instruction development, dynamic reconfiguration, and integration with machine learning, researchers can continue to enhance the performance and applicability of digital signal processing algorithms. These efforts will significantly contribute to the ongoing evolution of FPGA-based systems, enabling more efficient and powerful solutions for a wide range of applications in the field of electronics and embedded systems.

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Appendix A

FFT NIOS II C Code

```
#include <stdio.h>

#include <stdlib.h>

#include <math.h>

#include <stdint.h>

#include <time.h>

#include <system.h>

#include <alt_types.h>

#define FRACTIONAL_BITS 16

#define FIXED_POINT_SCALE (1 << FRACTIONAL_BITS)

// Helper functions to convert between float and fixed-point integer

int float_to_fixed(float f) {

    return (int)(f * FIXED_POINT_SCALE);

}

float fixed_to_float(int i) {

    return (float)i / FIXED_POINT_SCALE;

}

// Function to calculate FFT using DIT algorithm with custom instructions

void fft_custom(int* real, int* imag, int n) {
```

```

int i, j, k, m;

int step, stage;

int32 t t real, t imag, u real, u imag, w real, w imag, temp real, temp imag;

int angle_index, half_size;

// Bit-reversal permutation

int bits = (int)log2(n);

for (i = 0; i < n; i++) {
    j = 0;
    for (k = 0; k < bits; k++) {
        j <<= 1;
        j |= (i >> k) & 1;
    }
    if (j > i) {
        // Swap real parts
        temp_real = real[i];
        real[i] = real[j];
        real[j] = temp_real;

        // Swap imaginary parts
        temp_imag = imag[i];
        imag[i] = imag[j];
        imag[j] = temp_imag;
    }
}

```

```

}

// FFT_custom calculation using DIT
for (stage = 1; stage <= bits; stage++) {
    step = 1 << stage;
    half_size = step / 2;

    for (m = 0; m < half_size; m++) {
        angle_index = m * n / step;
        w_real = float_to_fixed(cos(-2 * M_PI * angle_index / n));
        w_imag = float_to_fixed(sin(-2 * M_PI * angle_index / n));

        for (i = m; i < n; i += step) {
            j = i + half_size;

            // Compute the multiplication results first

            int32_t scaled_w_real_realj = ALT_CI_MULTIPLIER(w_real, real[j]) /
FIXED_POINT_SCALE;

            int32_t scaled_w_imag_imagj = ALT_CI_MULTIPLIER(w_imag, imag[j]) /
FIXED_POINT_SCALE;

            int32_t scaled_w_real_imagj = ALT_CI_MULTIPLIER(w_real, imag[j]) /
FIXED_POINT_SCALE;

            int32_t scaled_w_imag_realj = ALT_CI_MULTIPLIER(w_imag, real[j]) /
FIXED_POINT_SCALE;

            // Compute x0

```

```
int16_t data_a3 = (scaled_w_imag_realj << 21) | (scaled_w_real_realj << 10) | (real[i]
& 0x3FF);
```

```
int16_t data_b3 = (scaled_w_imag_imagj << 21) | (scaled_w_real_imagj << 10) |
(imag[i] & 0x3FF);
```

```
int32_t result3 = __builtin_custom_inii(ALT_CI_X0_0_N, data_a3, data_b3);
```

```
// Extract the results for calculate_X0
```

```
int16_t real_i = (result3 >> 16) & 0xFFFF;
```

```
int16_t imag_i = result3 & 0xFFFF;
```

```
// Compute x1
```

```
int16_t data_a4 = (scaled_w_imag_realj << 21) | (scaled_w_real_realj << 10) | (real[i]
& 0x3FF);
```

```
int16_t data_b4 = (scaled_w_imag_imagj << 21) | (scaled_w_real_imagj << 10) |
(imag[i] & 0x3FF);
```

```
int32_t result4 = __builtin_custom_inii(ALT_CI_X1_0_N, data_a4, data_b4);
```

```
// Extract the results for calculate_X1
```

```
int16_t real_j = (result4 >> 16) & 0xFFFF;
```

```
int16_t imag_j = result4 & 0xFFFF;
```

```
// Update real and imag arrays using results from custom instructions
```

```
real[i] = real_i;
```

```
imag[i] = imag_i;
```

```
real[j] = real_j;
```

```
imag[j] = imag_j;
```

```

    }
}
}
}

```

// Function to calculate FFT using DIT algorithm without custom instructions (with added computational overhead)

```

void fft_software(int* real, int* imag, int n) {

    int i, j, k, m;

    int step, stage;

    double t_real, t_imag, u_real, u_imag, w_real, w_imag, temp_real, temp_imag;

    int angle_index, half_size;

    // Bit-reversal permutation

    int bits = (int)log2(n);

    for (i = 0; i < n; i++) {

        j = 0;

        for (k = 0; k < bits; k++) {

            j <<= 1;

            j |= (i >> k) & 1;

        }

        if (j > i) {

            // Swap real parts

            temp_real = real[i];

```

```

real[i] = real[j];
real[j] = temp_real;

// Swap imaginary parts
temp_imag = imag[i];
imag[i] = imag[j];
imag[j] = temp_imag;
}
}

// FFT software calculation using DIT
for (stage = 1; stage <= bits; stage++) {
    step = 1 << stage;
    half_size = step / 2;

    for (m = 0; m < half_size; m++) {
        angle_index = m * n / step;
        w_real = cos(-2 * M_PI * angle_index / n);
        w_imag = sin(-2 * M_PI * angle_index / n);

        for (i = m; i < n; i += step) {
            j = i + half_size;

            // Compute t_real and t_imag

```

```

int32_t w_real_realj = w_real * real[j];
int32_t w_imag_imagj = w_imag * imag[j];
int32_t w_real_imagj = w_real * imag[j];
int32_t w_imag_realj = w_imag * real[j];

t_real = w_real_realj - w_imag_imagj;
t_imag = w_real_imagj + w_imag_realj;

// Compute u_real and u_imag
u_real = real[i];
u_imag = imag[i];

// Update real and imag arrays
real[i] = u_real + t_real;
imag[i] = u_imag + t_imag;
real[j] = u_real - t_real;
imag[j] = u_imag - t_imag;
}
}
}
}

int main() {

```

```

int n, i;

printf("Enter the length of the FFT (must be a power of 2): ");

scanf("%d", &n);

int* real = (int*)malloc(n * sizeof(int));

int* imag = (int*)malloc(n * sizeof(int));

int* real_copy = (int*)malloc(n * sizeof(int));

int* imag_copy = (int*)malloc(n * sizeof(int));

if (real == NULL || imag == NULL || real_copy == NULL || imag_copy == NULL) {

    printf("Memory allocation failed\n");

    return -1;

}

// Get user-defined values for real and imaginary parts

printf("Enter the real and imaginary parts for each input:\n");

for (i = 0; i < n; i++) {

    printf("Input %d:\n", i);

    printf("Real part: ");

    scanf("%d", &real[i]);

    printf("Imaginary part: ");

    scanf("%d", &imag[i]);

    real_copy[i] = real[i]; // Copy for software-only FFT

```

```

    imag_copy[i] = imag[i]; // Copy for software-only FFT
}

// Measure time for FFT with custom instructions

clock_t start_custom = clock();

fft_custom(real, imag, n);

clock_t end_custom = clock();

double time_spent_custom = (double)(end_custom - start_custom) / CLOCKS_PER_SEC;

printf("FFT result with custom instructions:\n");

for (i = 0; i < n; i++) {
    printf("X[%d] = %d + %di\n", i, real[i], imag[i]);
}

printf("Time taken to compute FFT with custom instructions: %f seconds\n",
time_spent_custom);

// Measure time and clock cycles for software-only FFT

clock_t start_software = clock();

fft_software(real_copy, imag_copy, n);

clock_t end_software = clock();

double time_spent_software = (double)(end_software - start_software) /
CLOCKS_PER_SEC;

printf("FFT result with software-only implementation:\n");

for (i = 0; i < n; i++) {
    printf("X[%d] = %d + %di\n", i, real_copy[i], imag_copy[i]);
}

```

```
}
```

```
    printf("Time taken to compute FFT with software-only implementation: %f seconds\n",  
time_spent_software);
```

```
    printf("Time taken to compute FFT with custom instructions: %f seconds\n",  
time_spent_custom);
```

```
printf("\nPerformance Comparison:\n");
```

```
printf("-----\n");
```

```
printf(" | Implementation          | Execution Time      |\n");
```

```
printf("-----\n");
```

```
printf(" | Custom Instructions      | %f                |\n", time_spent_custom);
```

```
printf("-----\n");
```

```
printf(" | Software-only Implementation | %f                |\n", time_spent_software);
```

```
printf("-----\n");
```

```
free(real);
```

```
free(imag);
```

```
free(real_copy);
```

```
free(imag_copy);
```

```
return 0;
```

```
}
```